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NEEDS Simulation-ready Compact Models

Tianshi Wang

A. Gokcen Mahmutoglu

Archit Gupta

Jaijeet Roychowdhury

EECS Department, University of California, Berkeley



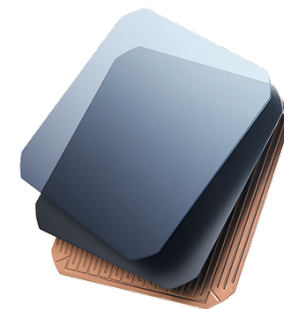
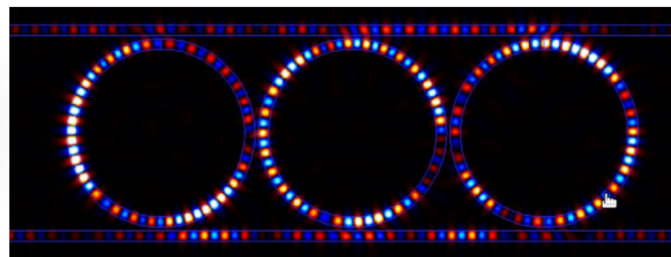
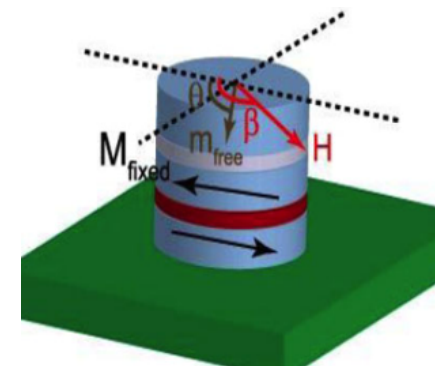
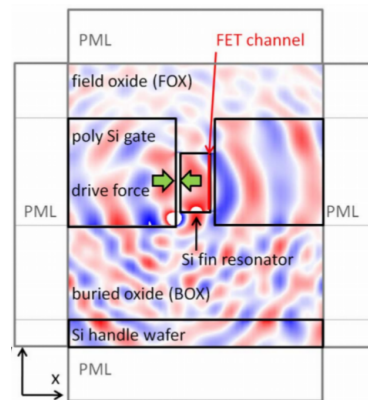
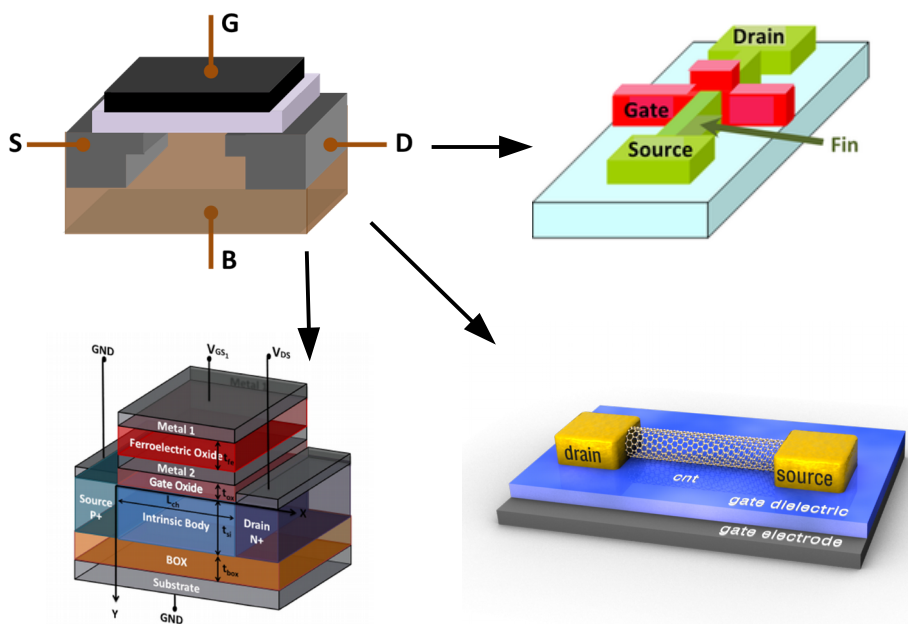
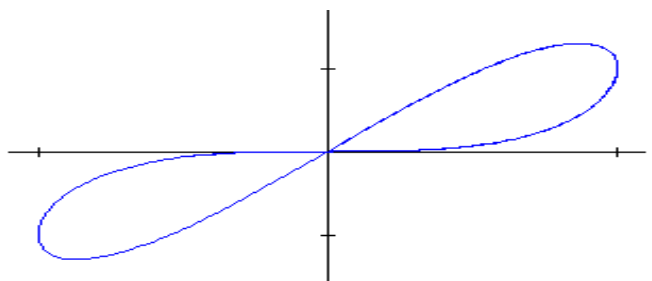
Compact Models for Simulation



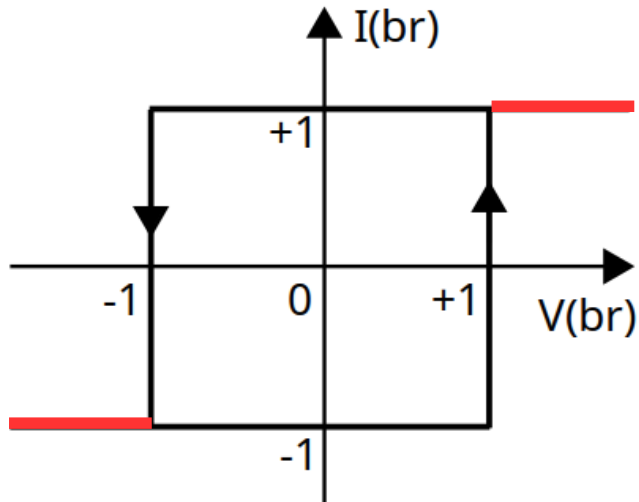
memristor
(RRAM, CBRAM, PCM...)



Applications:
computation
communication
energy systems



Compact Models for Simulation



not

“memory state”
“hidden state”

```

1 real i;
2 analog begin
3     if V(br) < -1
4         i = -1;
5     if V(br) > +1
6         i = +1;
7     I(br) <+ i;
8 end
    
```

not an analog
compact model

```

$bound_step(tstep);
c_time = $abstime;
dt = c_time - p_time;
x = x_last + dt * exp(...);
    
```

```

$rdist_normal(rand_seed, 0);
    
```

```

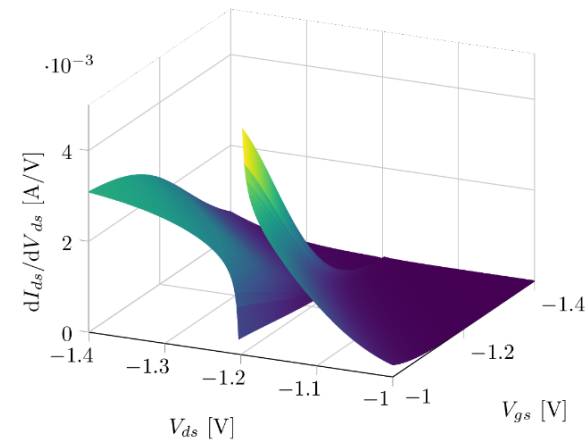
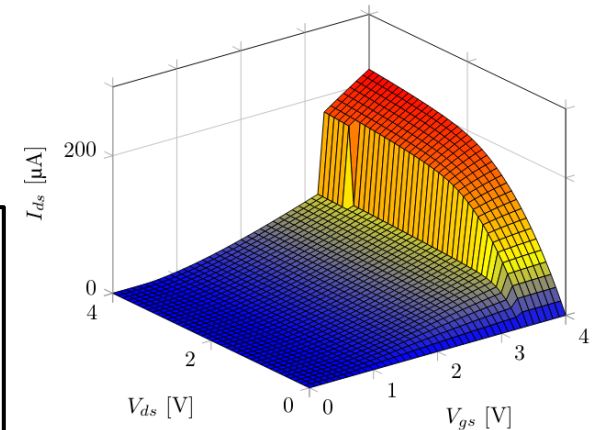
@(initial_step) begin
    x = x_init;
end
    
```

only for TRAN
none works for DC, AC, PSS

```

1 int isON = 0;
2 if (abs(V(...)) > V_snap)
3     isON = 1;
4 if (isON) {
5     ...
6 } else {
7     ...
8 }
    
```

Boolean variable
“hybrid model”



Good Compact Models

- “simulation-ready”

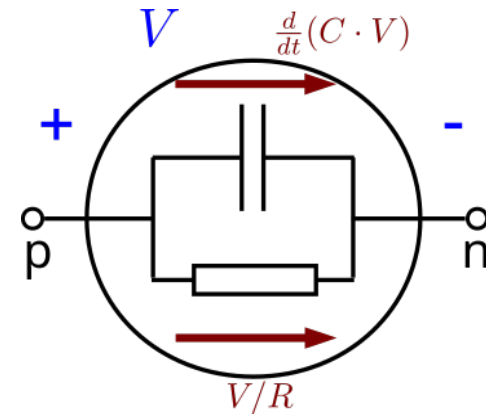
- run in all analyses (DC/AC/TRAN/sensitivity/shooting/HB/...)
- run in all simulators

consistently

~~analysis-specific code~~

- a simple (trivial) example

```
...  
I(p, n) <+ V(p, n)/R;  
I(p, n) <+ ddt(C * V(p, n));  
...
```



- differential equation format

$$ipn = \frac{d}{dt}q(vpn) + f(vpn)$$

“charges” and “currents”, continuous and smooth

- no \$abstime, idt(), @initial_step, @cross, \$bound_step, \$rdist_normal etc.
- well-posed

Mahmutoglu/Wang/Gupta/Roychowdhury (2017) "Well-Posed Device Models for Electrical Circuit Simulation"

Good Compact Models

- Well-posedness: https://en.wikipedia.org/wiki/Well-posed_problem
 - a solution exists
 - the solution is unique
 - the solution's behavior changes continuously with the initial conditions.

original definition applies to problems/analyses, not models
- finite and unique outputs
 - $1/(x-a)$, $\log(x)$, $\text{sqrt}(x)$, ...
 - random number generation for noise and variability?
- continuous and smooth
 - C^∞ : higher-order derivatives for PSS, distortion, homotopy
- input range
 - *should a model evaluate at 1000V?*
- higher-level requirements
 - well-understood physics, well-formulated (in DAE), well-tested
 - well-written in Verilog-A

Good Verilog-A Practices

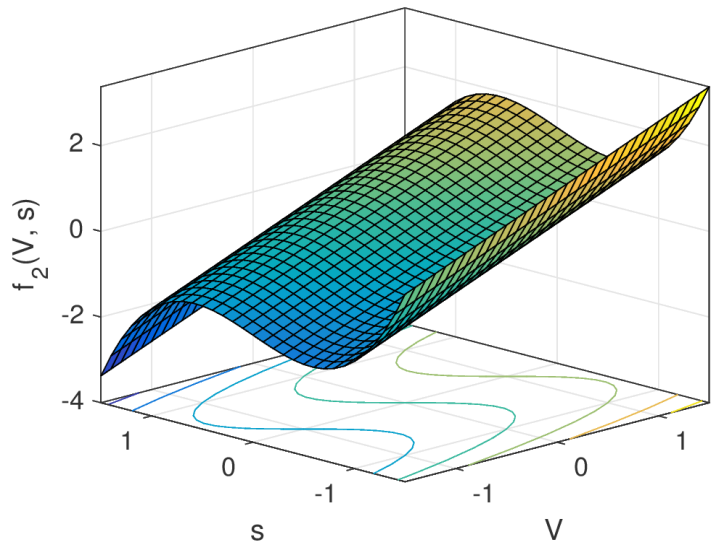
- DO use branches.
- DO declare and initialize all variables and DO NOT use memory states.
- DO NOT use event control statements.
- DO NOT use analysis dependent functions.
- DO use ddt, but only in allowed ways.
- DO NOT use idt.
- DO NOT use time-varying functions.
- DO NOT use random number generators.
- DO take great care when using implicit equations.
- DO NOT allow any nodes in your model without having at least one branch with a well-defined contribution attached to it.
- DO NOT use bias-dependent switch branch and node collapse conditions.
- DO use parameter ranges.

[Colin McAndrew et al, "Best Practices for Compact Modeling in Verilog-A"](#)

[Geoffrey Coram, "How to \(and how not to\) write a compact model in Verilog-A"](#)

[A.G. Mahmutoglu et al, "Well-Posed Device Models for Electrical Circuit Simulation"](#)

Case Study: Devices with Hysteresis

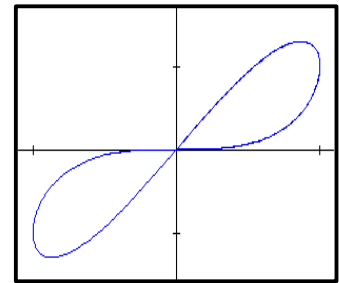
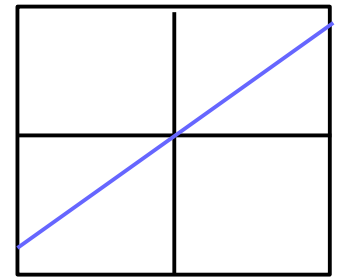


$$\text{ipn} = f(\text{vpn})$$

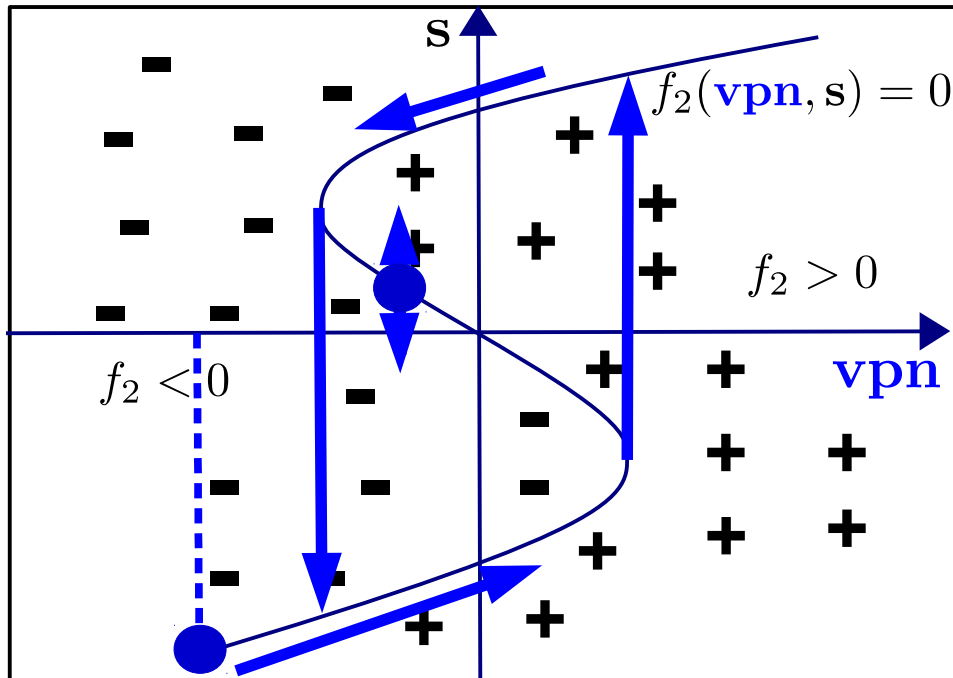


$$\text{ipn} = f_1(\text{vpn}, s)$$

$$\frac{d}{dt}s = f_2(\text{vpn}, s)$$



internal state variable
"memory"



Example:

$$f_1(\text{vpn}, s) = \frac{\text{vpn}}{R} \cdot (1 + \tanh(s))$$

$$f_2(\text{vpn}, s) = \text{vpn} - s^3 + s$$

hysteresis \neq discontinuity or if-else

hysteresis \neq \$abstime, \neq hybrid models

Case Study: Devices with Hysteresis

Template:

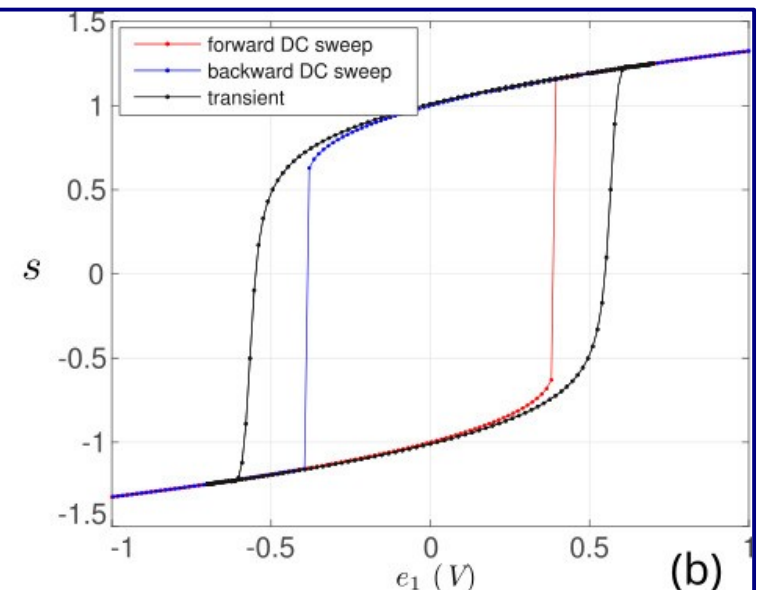
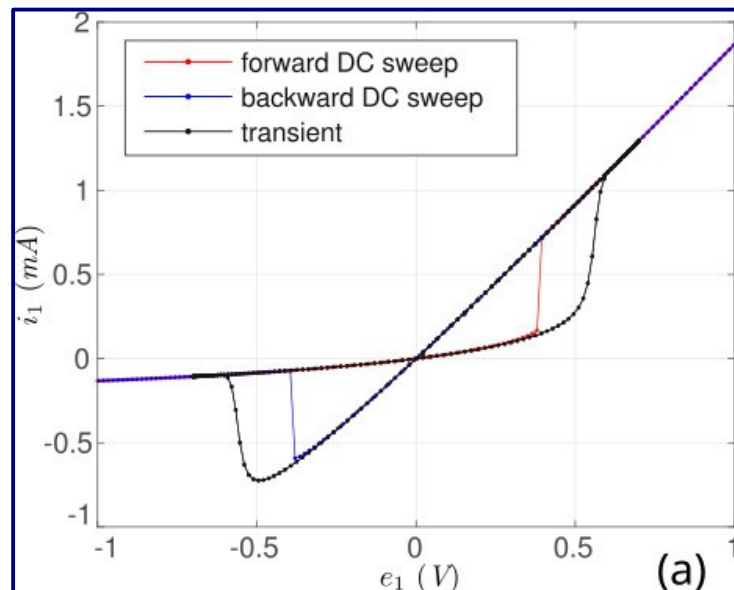
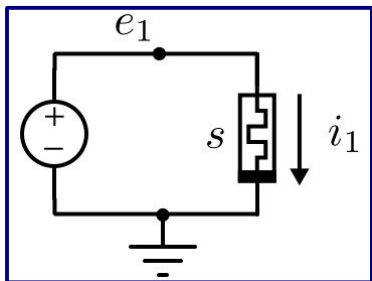
$$i_{pn} = f_1(v_{pn}, s)$$

$$\frac{d}{dt}s = f_2(v_{pn}, s)$$

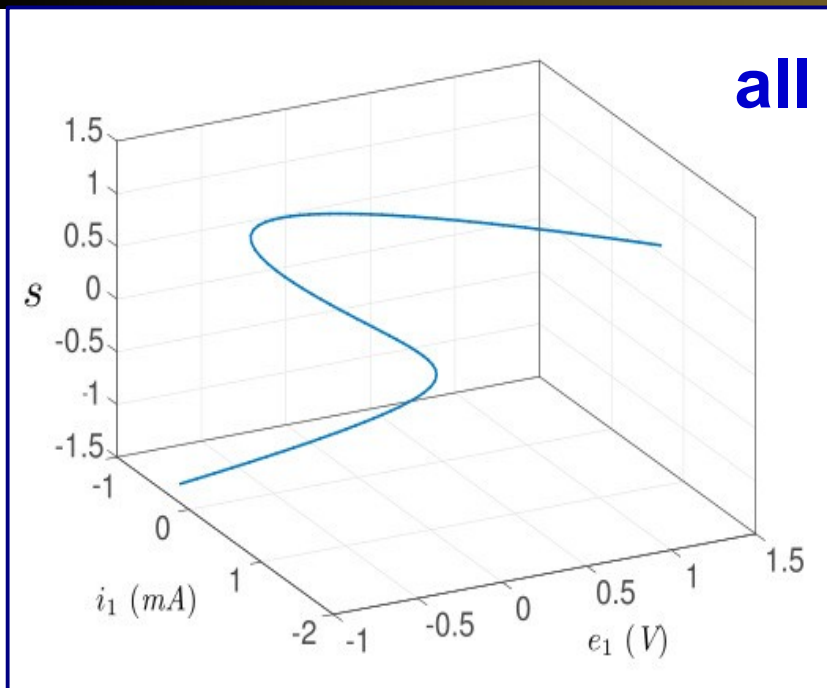
MAPP:

$$i_{pn} = \frac{d}{dt} \underbrace{q_e(v_{pn}, s)}_{\mathbf{0}} + \underbrace{f_e(v_{pn}, s)}_{f_1}$$

$$0 = \frac{d}{dt} \underbrace{q_i(v_{pn}, s)}_{-s} + \underbrace{f_i(v_{pn}, s)}_{f_2}$$

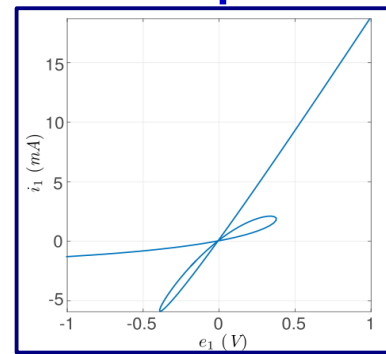


Case Study: Devices with Hysteresis

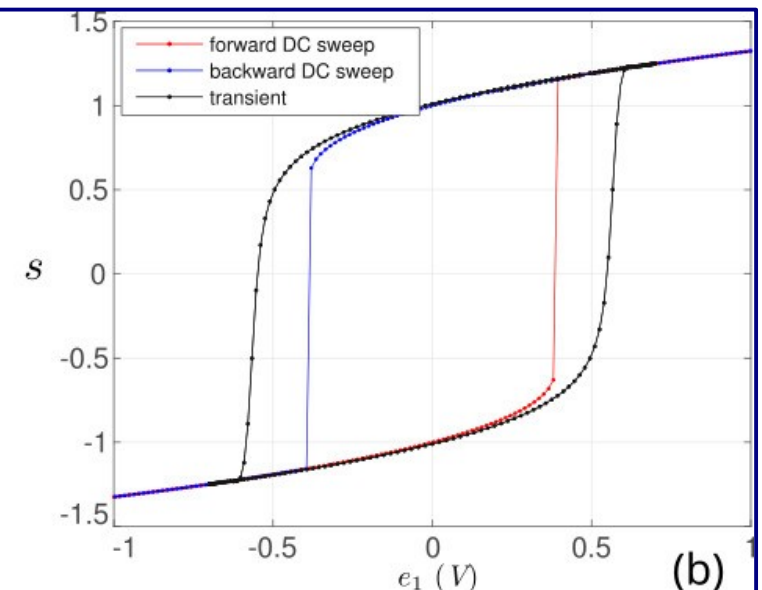
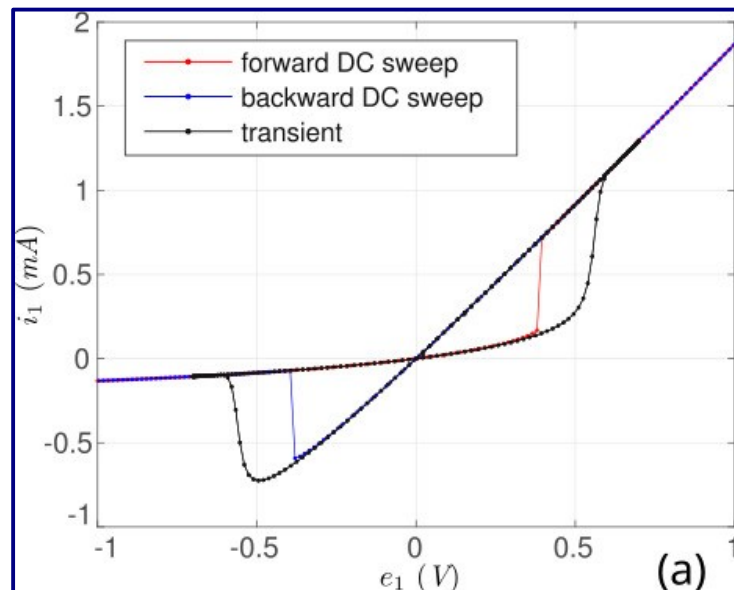
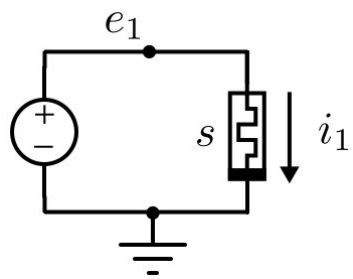
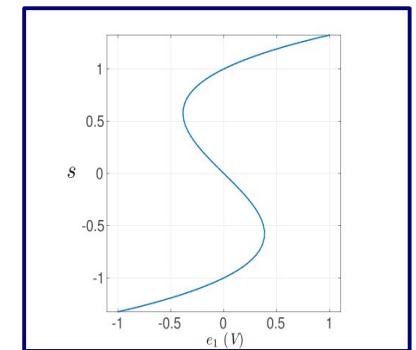


all DC sols from homotopy analysis
(like a curve tracer)

top



side



Internal Unknowns in Verilog-A

$$\text{ipn} = \frac{\text{vpn}}{R} \cdot (1 + \tanh(s))$$

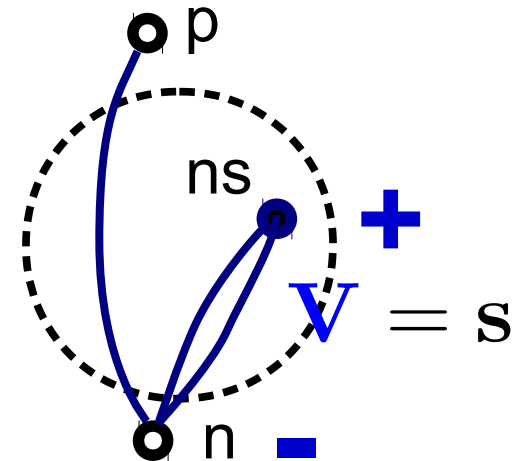
$$\frac{d}{dt}(\tau \cdot s) = \text{vpn} - s^3 + s \quad \leftarrow \text{use a potential or flow}$$

```

1 `include "disciplines.vams"
2 module hys(p, n);
3   inout p, n;
4   electrical p, n, ns;
5   branch (ns, n) ns_br1;
6   branch (ns, n) ns_br2;
7   parameter real R = 1e3 from (0:inf);
8   parameter real k = 1 from (0:inf);
9   parameter real tau = 1e-5 from (0:inf);
10  real s;
11
12  analog begin
13    s = V(ns, n);
14    I(p, n) <+ V(p, n)/R * (1+tanh(k*s));
15    I(ns_br1) <+ V(p, n) - pow(s, 3) + s;
16    I(ns_br2) <+ ddt(-tau*s);
17  end
18 endmodule

```

internal node

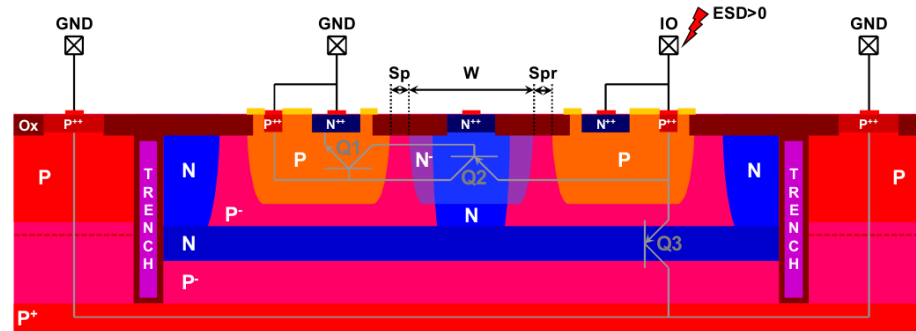


internal unknown

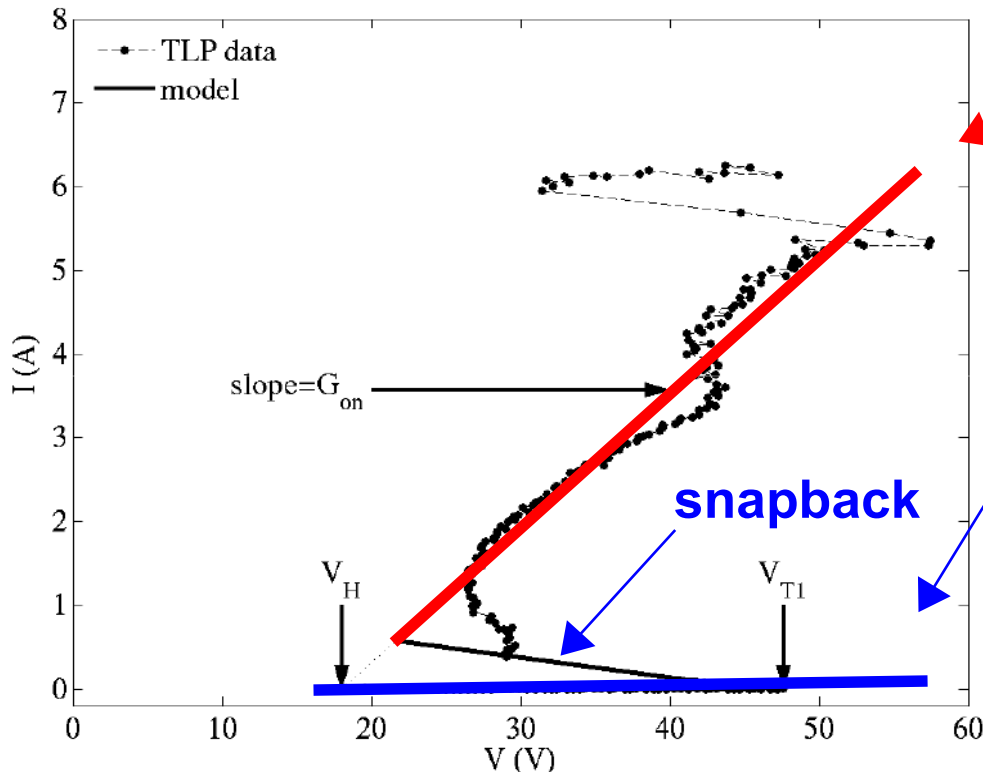
implicit differential equation

ESD Snapback Model

ESD protection device



Gendron, et al. "New High Voltage ESD Protection Devices based on Bipolar Transistors for Automotive Applications." IEEE EOS/ESD Symposium, 2011.



Ida/McAndrew. "A Physically-based Behavioral Snapback Model." IEEE EOS/ESD Symposium, 2012.

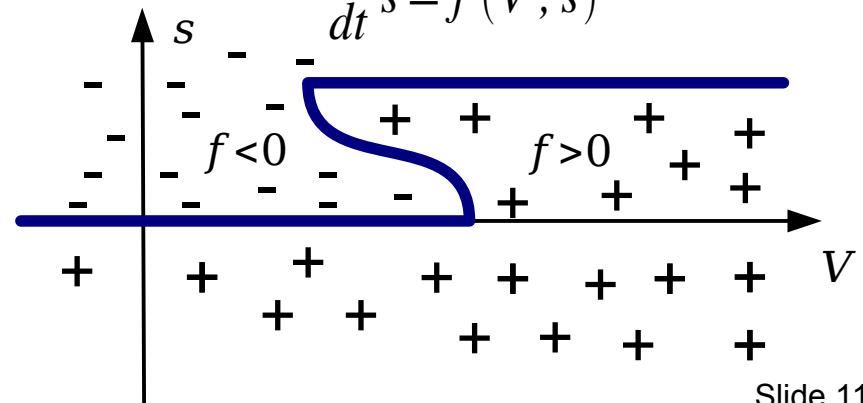
$$I_{on} = G_{on} \cdot (V - V_H)$$

$$I_{off} = I_S \cdot (1 - e^{-V/\phi_T}) \cdot \sqrt{1 + \frac{\max(V, 0)}{V_D}}$$

$$I = s \cdot I_{on} + I_{off}$$

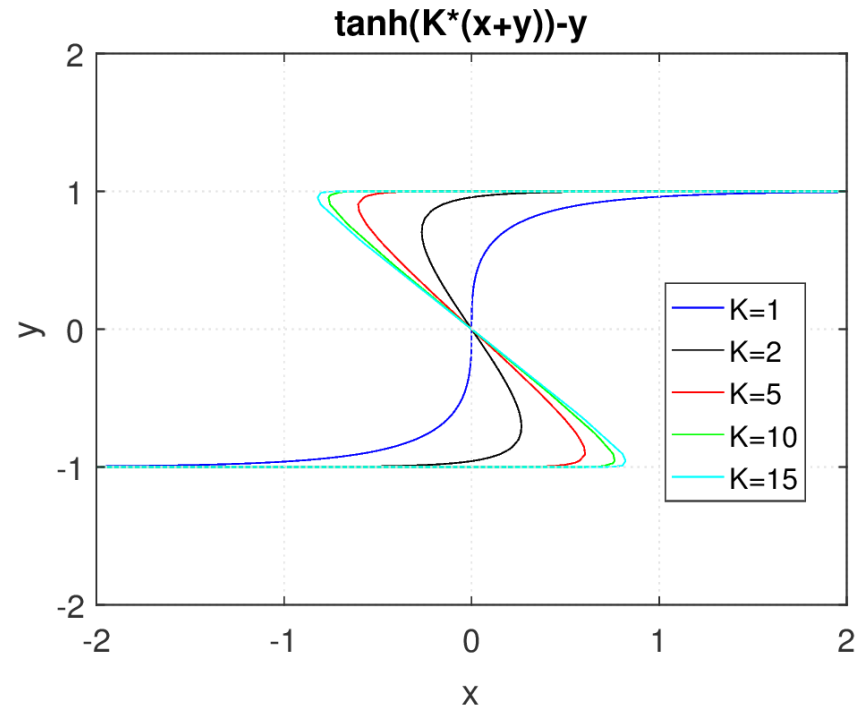
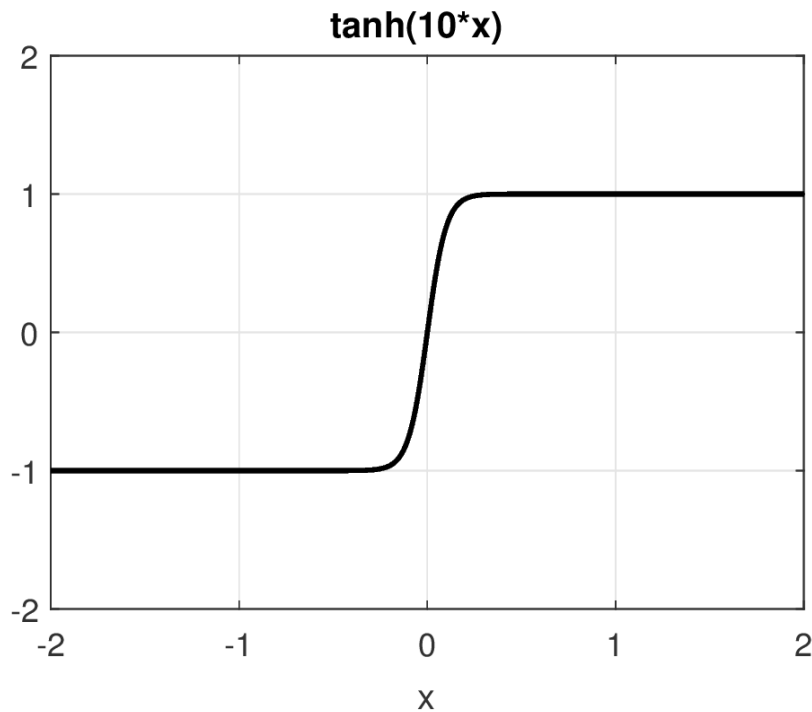
internal state: indicator of impact ionization

$$\frac{d}{dt} s = f(V, s)$$



ESD Snapback Model

$$\frac{d}{dt}s = f(V, s) \quad \text{many possible functions}$$



```
...  
Vstar = 2*(V(p, n)-0.5*VT1-0.5*VIH)/(VT1-VIH);  
sstar = 2*(s-0.5);  
I(ns, n) <+ tanh(K*(Vstar + sstar)) - sstar;  
...
```

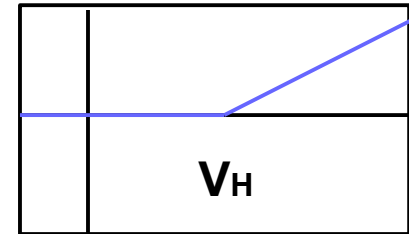
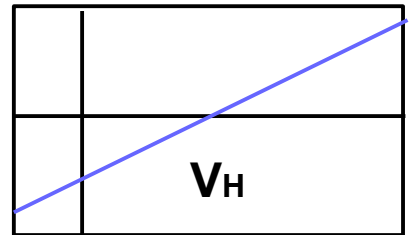
**shift transition points
shift range to (0, 1)**

ESD Snapback Model

```
1 `include "disciplines.vams"
2
3 module ESDclamp(p, n);
4     inout p, n;
5     electrical p, n, ns;
6
7     parameter real Gon = 0.1 from (0:inf);
8     ...
9
10    analog begin
11        s = V(ns, n);
12        Ion = smoothclip(Gon*(V(p, n)-VH), smoothing)
13              - smoothclip(-Gon*VH, smoothing);
14        Ioff = Is * (1 - limexp(-V(p, n)/VT))
15                * sqrt(1 + max(V(p, n), 0)/VD);
16        I(p, n) <+ Ioff + pow(s, Alpha) * Ion;
17        I(p, n) <+ ddt(C * V(p, n));
18
19        Vstar = 2*(V(p, n)-0.5*VT1-0.5*VIH)/(VT1-VIH);
20        sstar = 2*(s-0.5);
21        I(ns, n) <+ tanh(K*(Vstar + sstar)) - sstar;
22        I(ns, n) <+ ddt(-tau*s);
23    end
24 endmodule
```

internal unknown
as a voltage

I_{on}



I_{off}

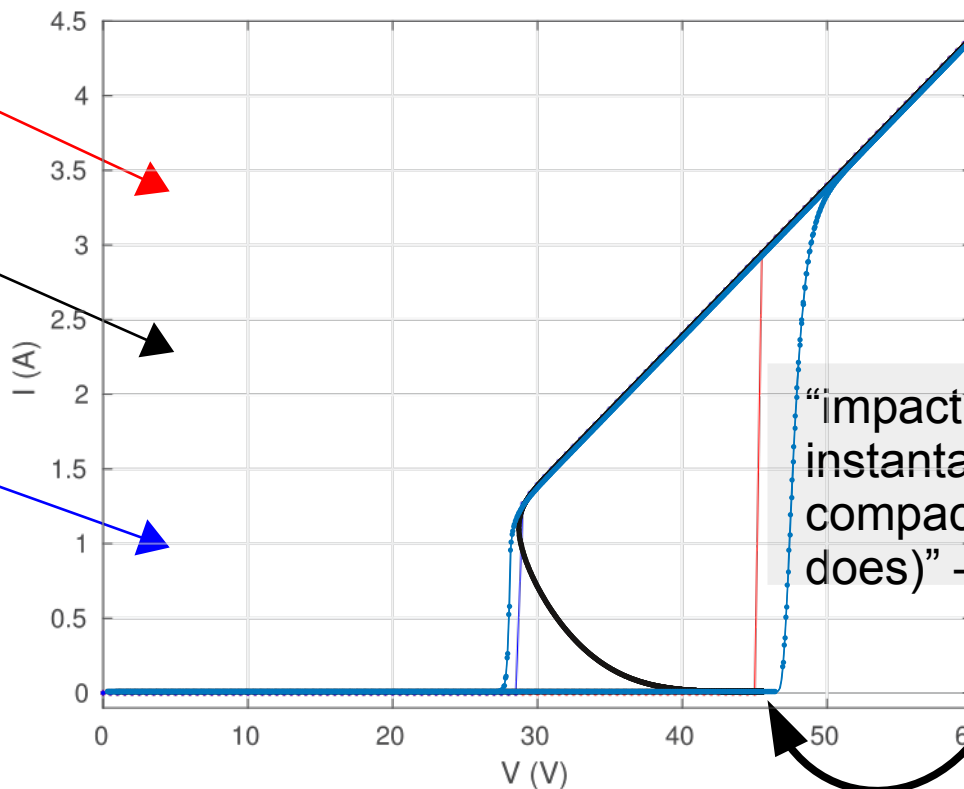
implicit
differential
equation

ESD Snapback Model

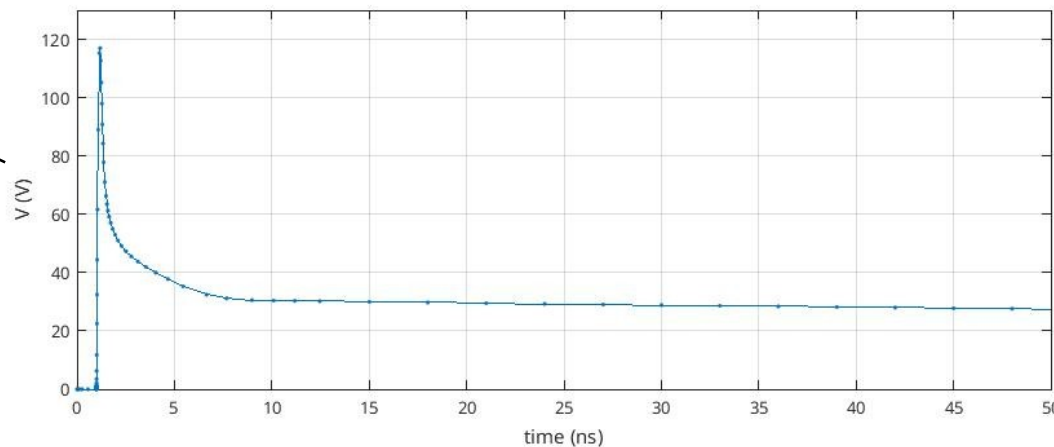
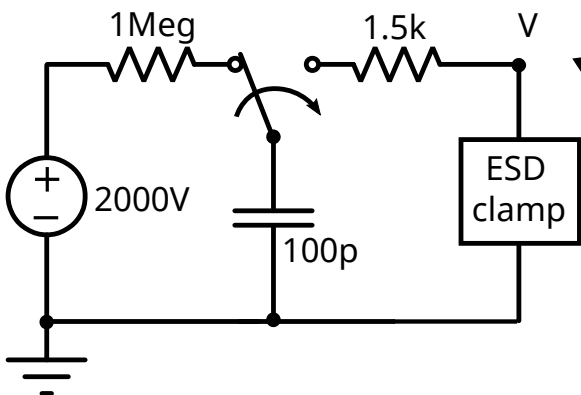
forward/backward
DC sweeps

homotopy
(all DC sols)

transient
voltage sweeps

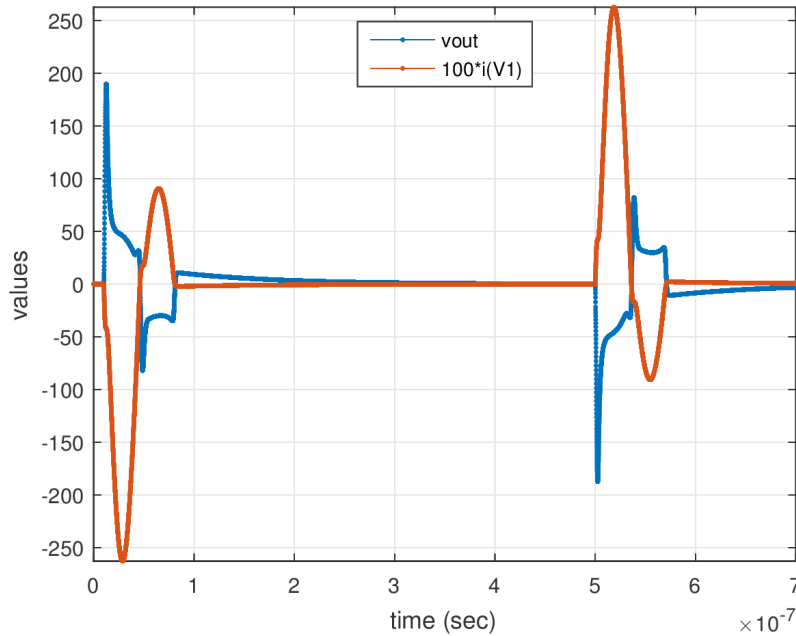


Human Body Mode (HBM) test

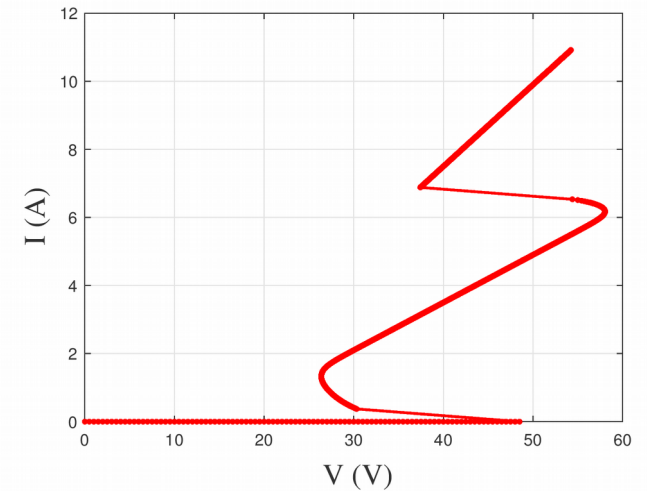
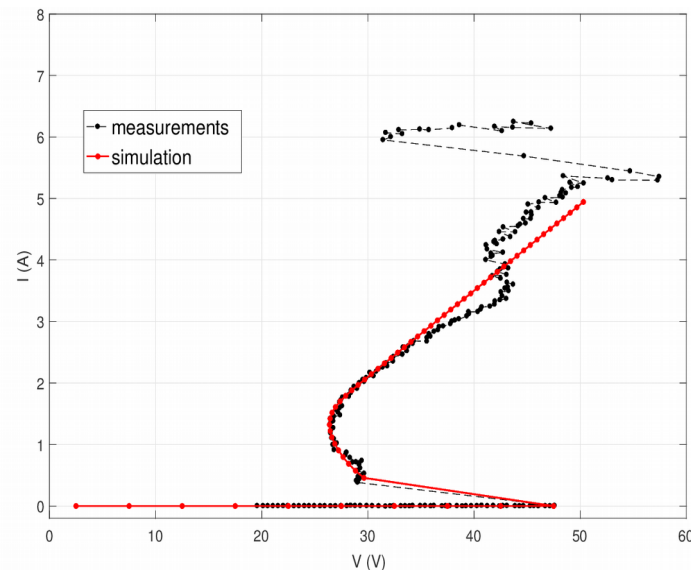
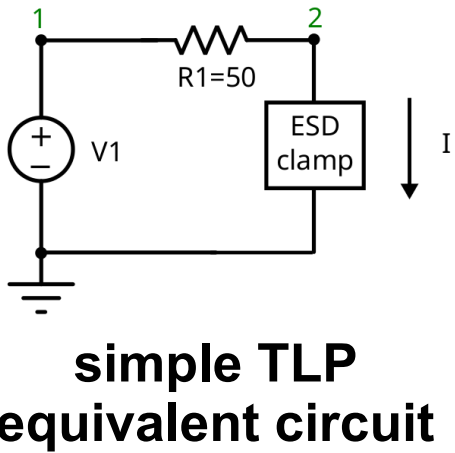
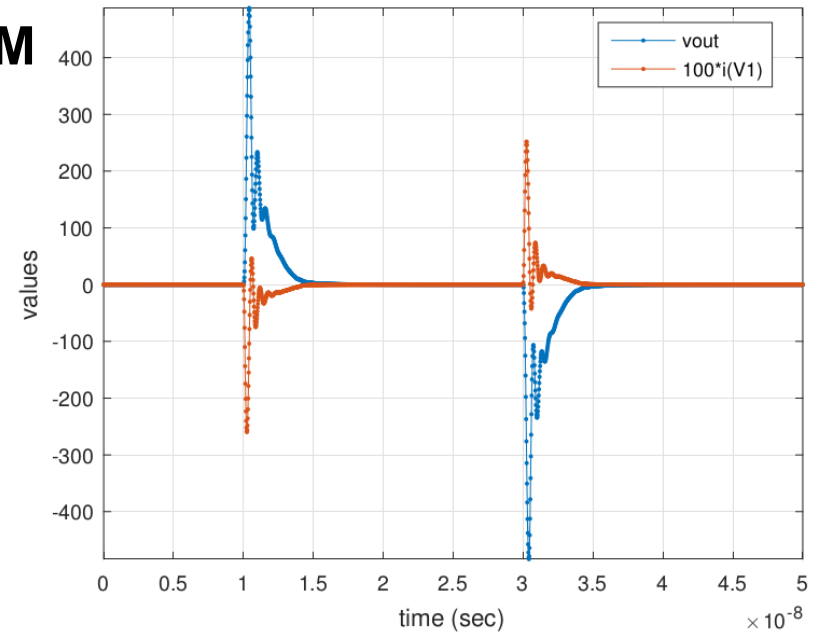


ESD Snapback Model

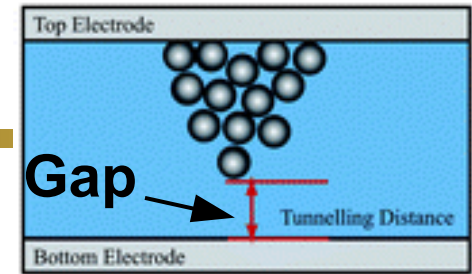
MM



CDM



RRAM Model



Template:

RRAM:

$$ipn = f_1(vpn, s)$$

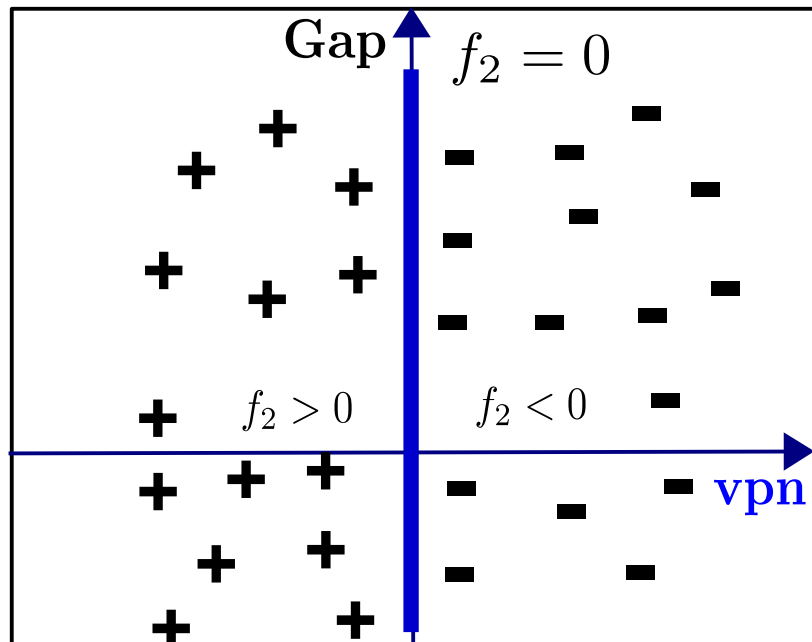
$$f_1(vpn, \text{Gap}) = I_0 \cdot e^{-\text{Gap}/g_0} \cdot \sinh(vpn/V_0)$$

$$\frac{d}{dt}s = f_2(vpn, s)$$

$$f_2(vpn, \text{Gap}) = -v_0 \cdot \exp\left(-\frac{E_a}{V_T}\right) \cdot \sinh\left(\frac{vpn \cdot \gamma \cdot a_0}{t_{ox} \cdot V_T}\right)$$

Jiang, Z., Wong, H. (2014). Stanford University Resistive-Switching Random Access Memory (RRAM) Verilog-A Model. nanoHUB.

$$\text{minGap} \leq \text{Gap} \leq \text{maxGap}$$



~~if gap < minGap
gap = minGap;~~

hybrid model

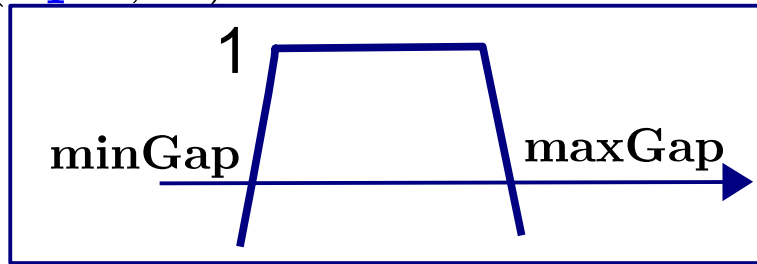
RRAM Model

Template:

RRAM:

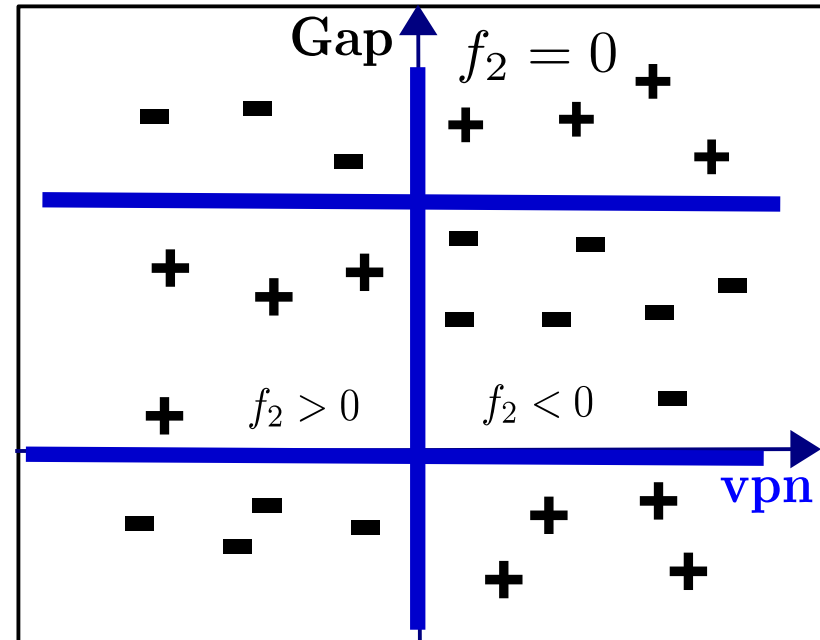
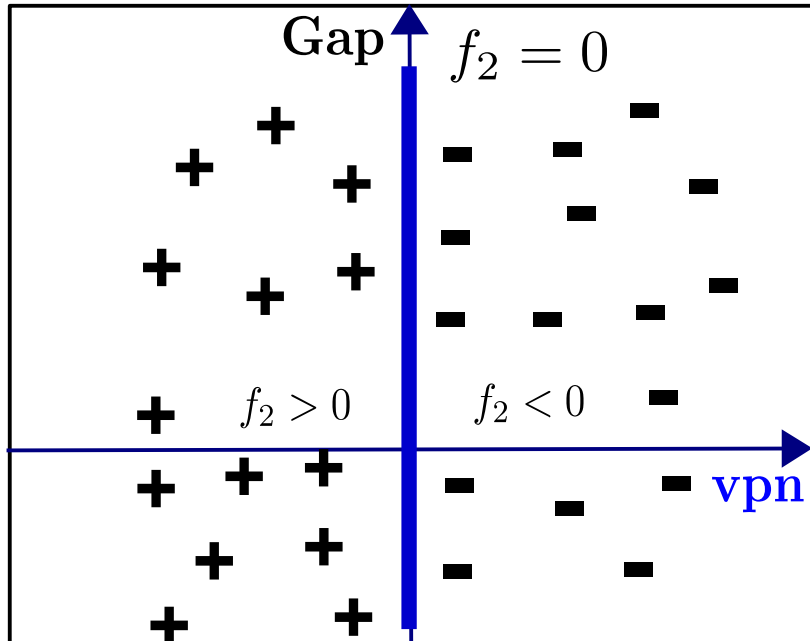
$$ipn = f_1(vpn, s) \quad f_1(vpn, Gap) = I_0 \cdot e^{-Gap/g^0} \cdot \sinh(vpn/V_0)$$

$$\frac{d}{dt}s = f_2(vpn, s) \quad f_2(vpn, Gap) = -v_0 \cdot \exp\left(-\frac{E_a}{V_T}\right) \cdot \sinh\left(\frac{vpn \cdot \gamma \cdot a_0}{t_{ox} \cdot V_T}\right)$$

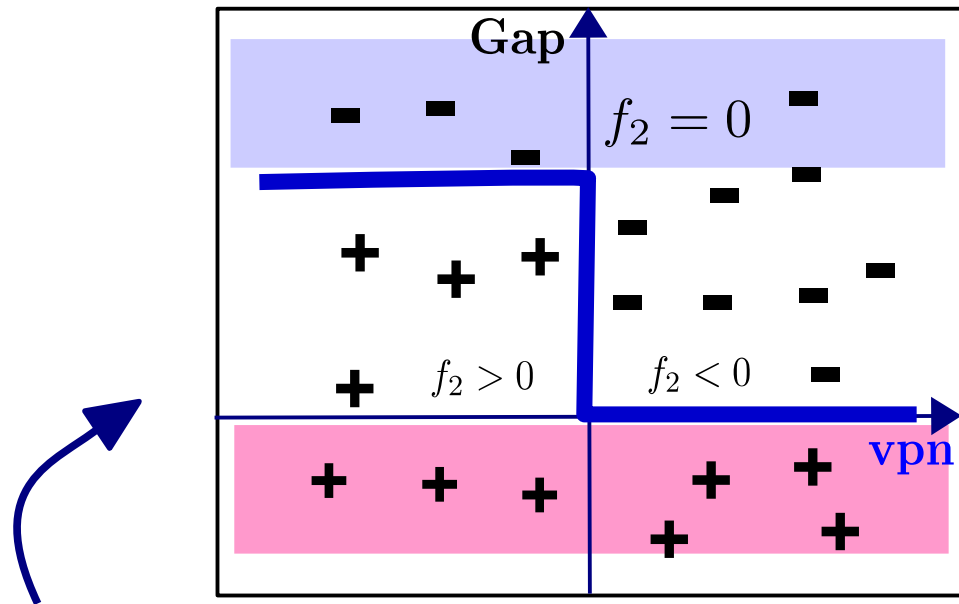


$$\times F_{window}(Gap)$$

Biolek, Jogelkar, Prodromakis, UMich, TEAM/VTEAM, Yakopcic, etc.

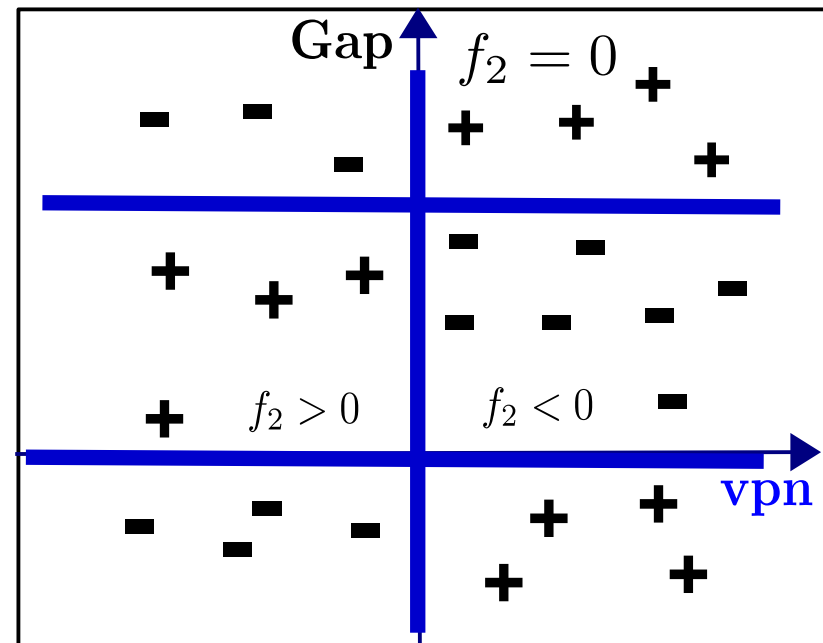
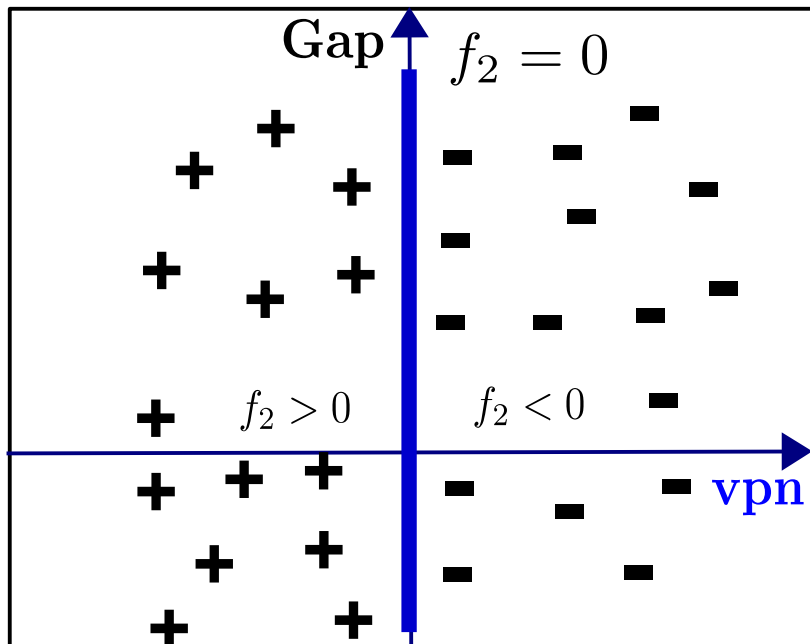


RRAM Model



clipping functions

Analogy: MEMS switch
Zener diode voltage regulator



Memristor Models

$$\frac{d}{dt}s = f_2(\mathbf{vpn}, s)$$

Available f2:

① linear ion drift

$$f_2 = \mu_v \cdot R_{on} \cdot f_1(\mathbf{vpn}, s)$$

② nonlinear ion drift

$$f_2 = a \cdot \mathbf{vpn}^m$$

③ Simmons tunnelling barrier

$$f_2 = \begin{cases} c_{off} \cdot \sinh\left(\frac{i}{i_{off}}\right) \cdot \exp\left(-\exp\left(\frac{s-a_{off}}{w_c} - \frac{i}{b}\right) - \frac{s}{w_c}\right), & \text{if } i \geq 0 \\ c_{on} \cdot \sinh\left(\frac{i}{i_{on}}\right) \cdot \exp\left(-\exp\left(\frac{a_{on}-s}{w_c} + \frac{i}{b}\right) - \frac{s}{w_c}\right), & \text{otherwise,} \end{cases}$$

④ TEAM model

⑤ Yakopcic model

⑥ Stanford/ASU

$$f_2 = -v_0 \cdot \exp\left(-\frac{E_a}{V_T}\right) \cdot \sinh\left(\frac{\mathbf{vpn} \cdot \gamma \cdot a_0}{t_{ox} \cdot V_T}\right)$$

$$\mathbf{ipn} = f_1(\mathbf{vpn}, s)$$

Available f1:

① $f_1 = (R_{on} \cdot s + R_{off} \cdot (1 - s))^{-1} \cdot \mathbf{vpn}$

② $f_1 = \frac{1}{R_{on}} \cdot e^{-\lambda \cdot (1-s)} \cdot \mathbf{vpn}$

③ $f_1 = s^n \cdot \beta \cdot \sinh(\alpha \cdot \mathbf{vpn}) + \chi \cdot (\exp(\gamma \cdot) - 1)$

④ $f_1 = \begin{cases} A_1 \cdot s \cdot \sinh(B \cdot \mathbf{vpn}), & \text{if } \mathbf{vpn} \geq 0 \\ A_2 \cdot s \cdot \sinh(B \cdot \mathbf{vpn}), & \text{otherwise.} \end{cases}$

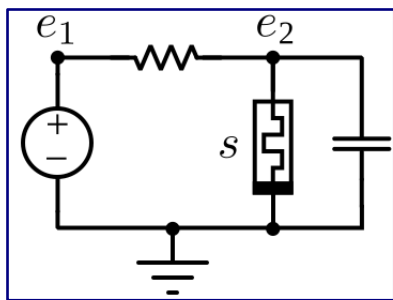
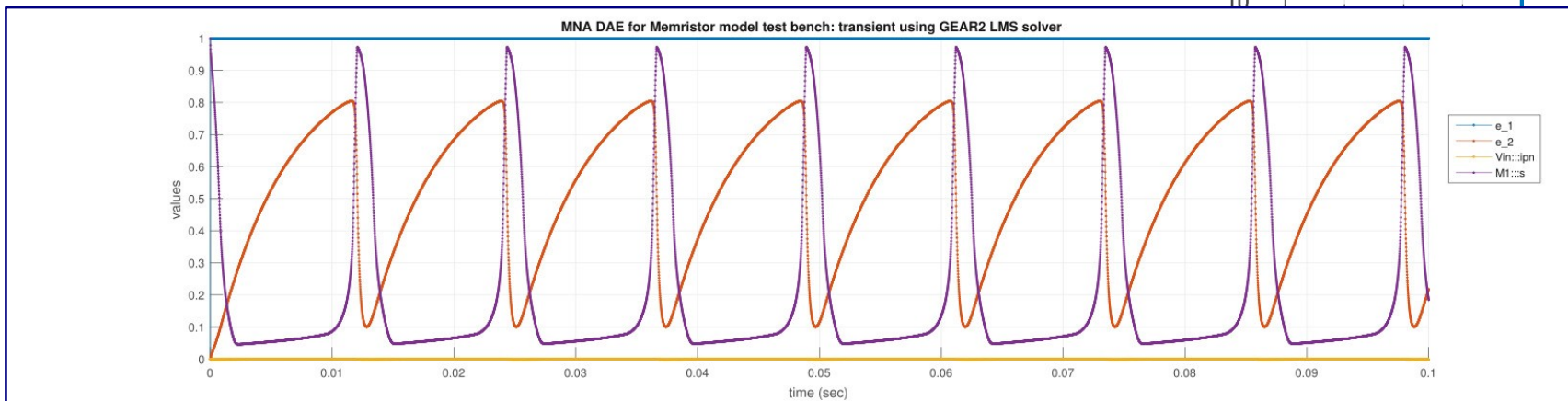
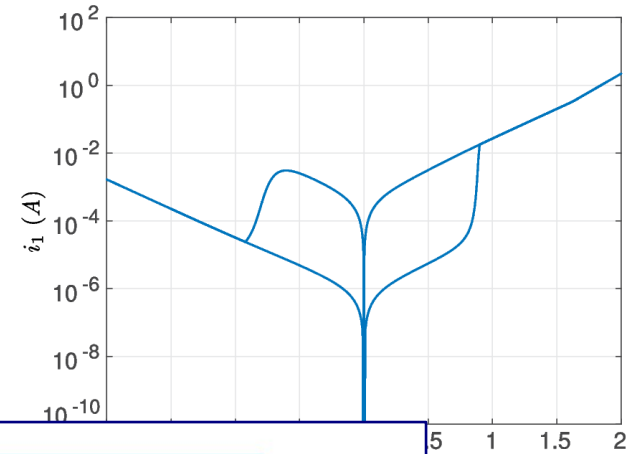
⑤ $f_1 = I_0 \cdot e^{-\text{Gap}/g_0} \cdot \sinh(\mathbf{vpn}/V_0)$
 $\text{Gap} = s \cdot \text{minGap} + (1 - s) \cdot \text{maxGap}.$

- set up boundary
- fix f2 flat regions
- smooth, safe funcs, scaling, etc.

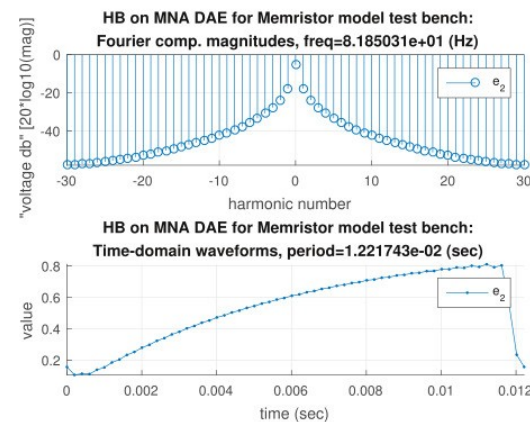
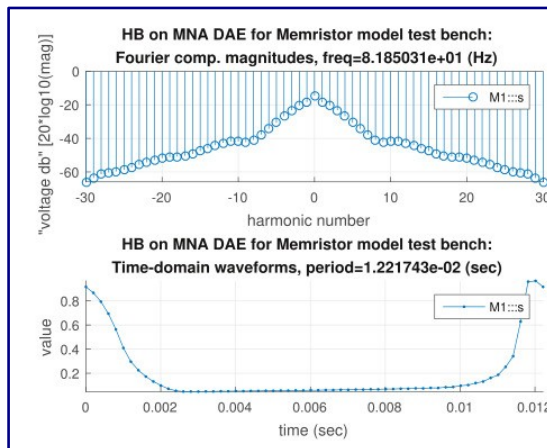
Memristor Models

A collection of models:

- all smooth, all well posed
- not just RRAM, but general memristive devices
- not just bipolar, but unipolar
- not just DC, AC, TRAN, but homotopy, PSS, ...



PSS using HB



Good Compact Models

- Well-posedness:
 - finite and unique outputs
 - continuous and smooth
 - input range
 - physics, DAE, tests, Verilog-A ...
- Good Verilog-A practices
 - [Geoffrey Coram, “How to \(and how not to\) write a compact model in Verilog-A”](#)
 - [Colin McAndrew et al, “Best Practices for Compact Modeling in Verilog-A”](#)
 - [A.G. Mahmutoglu et al, “Well-Posed Device Models for Electrical Circuit Simulation”](#)
- Case study with hysteretic devices
 - ESD snapback
 - RRAM/memristors