Boolean Computing using Oscillators

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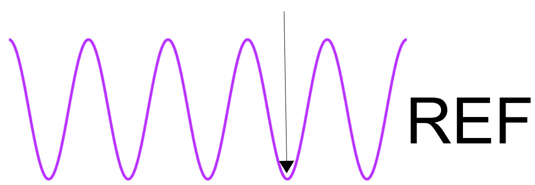
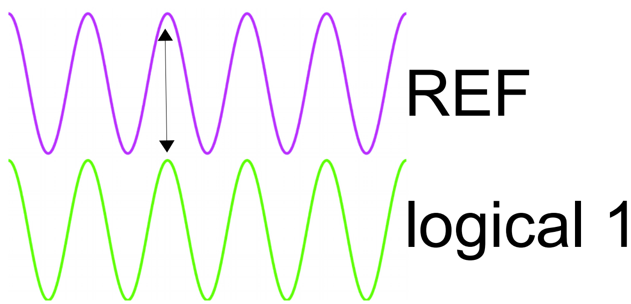
Encoding Bits Using Phase

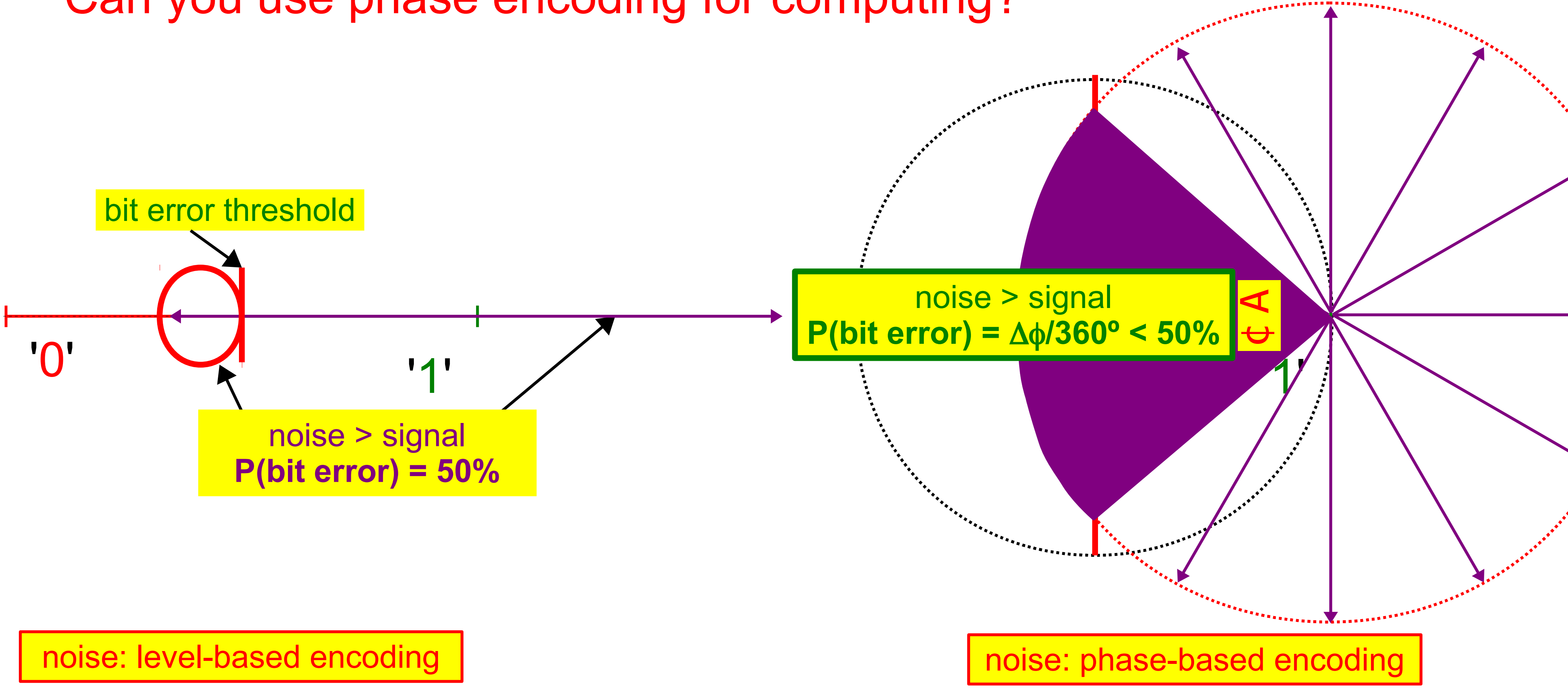




- How do you use this for computing?
- Even if you can: what is the advantage?

Superior Noise Immunity

- loose analogy: PM/FM vs AM in radio
- **Same reason why the BER of BPSK is superior to that of BASK**
- Can you use phase encoding for computing?

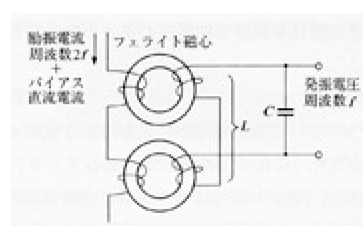


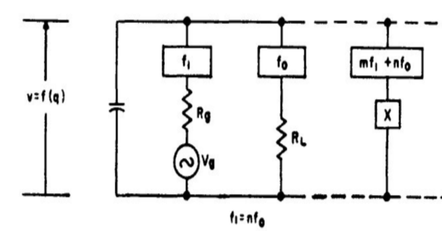
Phase Logic Computer: Eiichi Goto, John von Neumann, 1950s and 60s

- “cheap and reliable”
  - “widely used in Japan”
- not easy to miniaturise
  - inductors, iron cores
  - transistors/ICs dominated
    - level-based logic

<u>Phase Based Logic</u>:
underlying circuitry/components have been **<u>difficult to miniaturise</u>** or **<u>impractical for integration</u>**

Oi Electric
Parametron X-ℵ-01, 1964
Ferro-Electronic Calculator



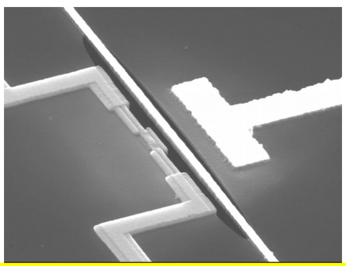


Key Result: (almost) Any Oscillator will Do

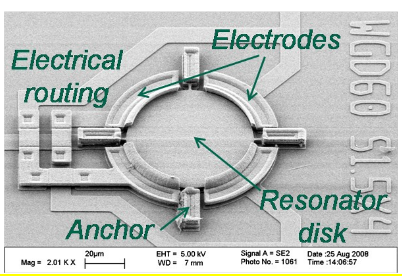
- **PHLOGON**: PHase LOGic using Oscillatory Nanosystems
  - details: J. Roychowdhury, “Boolean Computation Using Self-Sustaining Nonlinear Oscillators”, arXiv:1410.5016 [cs.ET], October 2014.

novel nanodevices

MEMS/NEMS

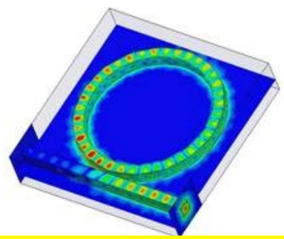


nanoswitch relaxation osc.



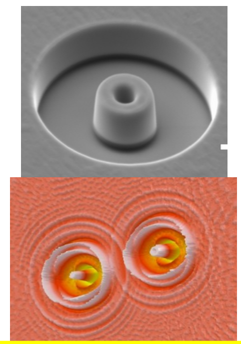
MEMS resonator osc.

opto-electronic

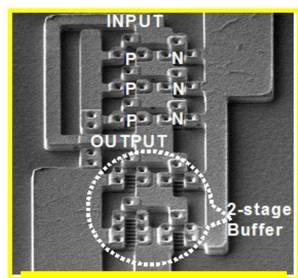


opto-resonator laser

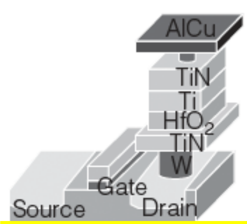
VCSELs



spin-torque

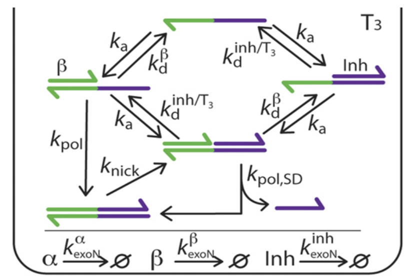


nanowire ring osc.

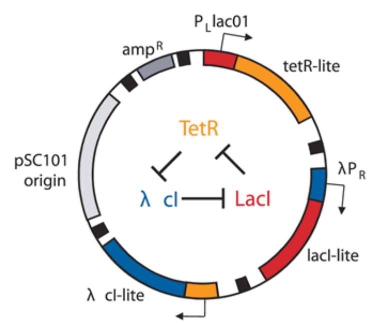


RRAM

synth. bio. (DNA)

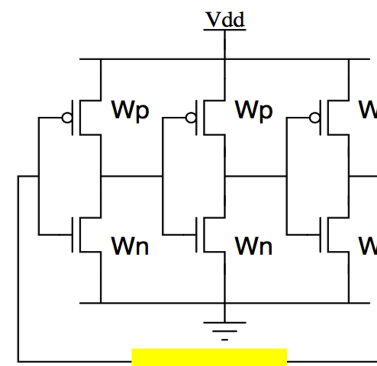


oligator

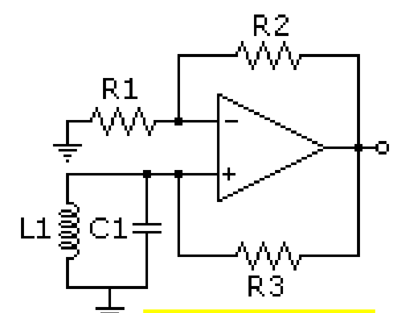


repressilator

CMOS/electronic



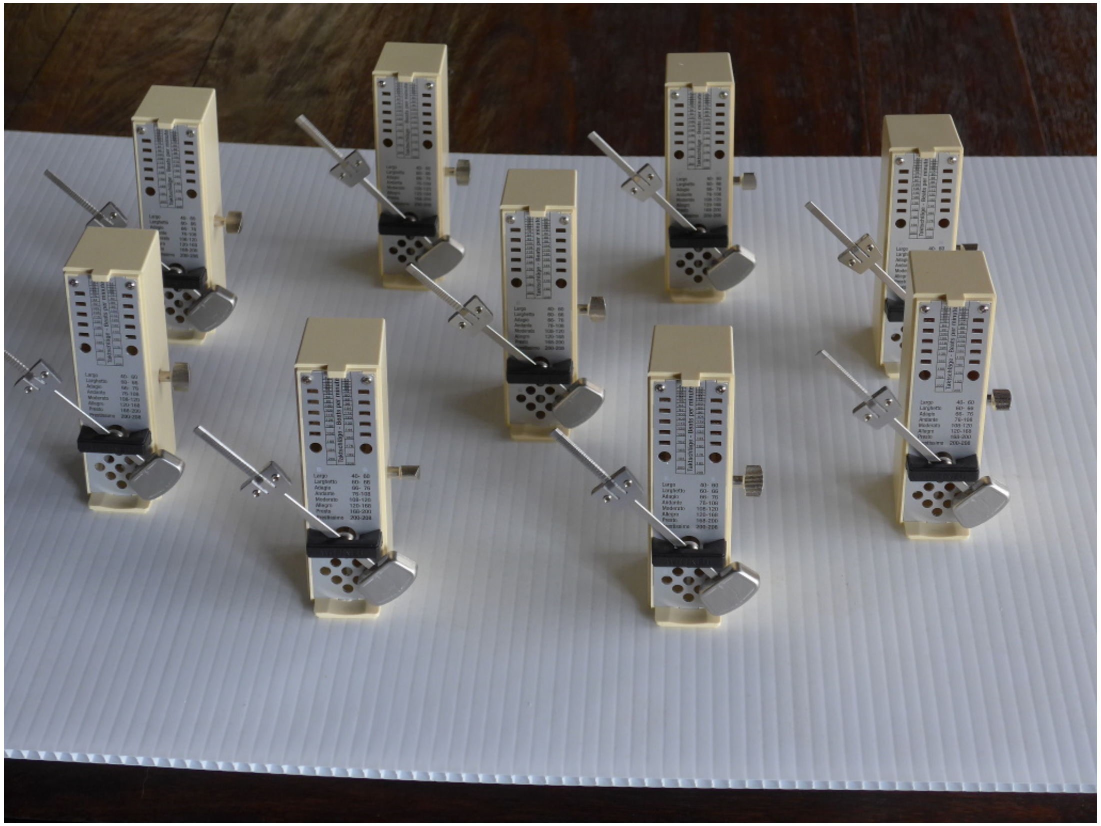
ring osc.



LC oscillator

Underlying Mechanism: Injection Locking

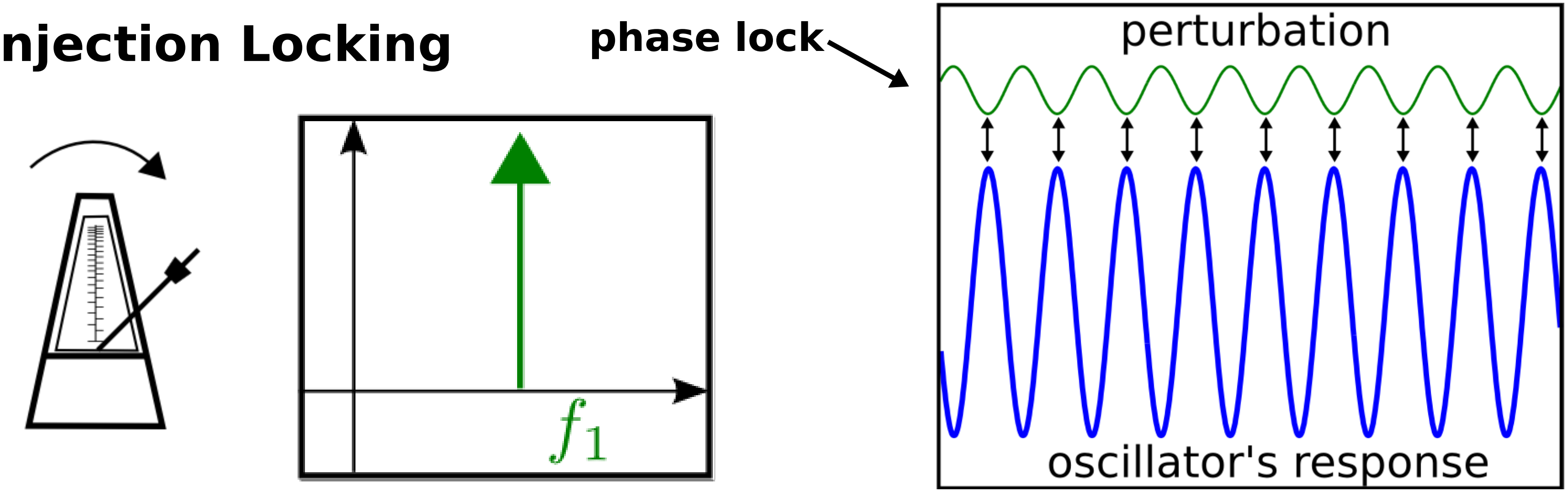
- Oscillators can synchronize in phase/frequency



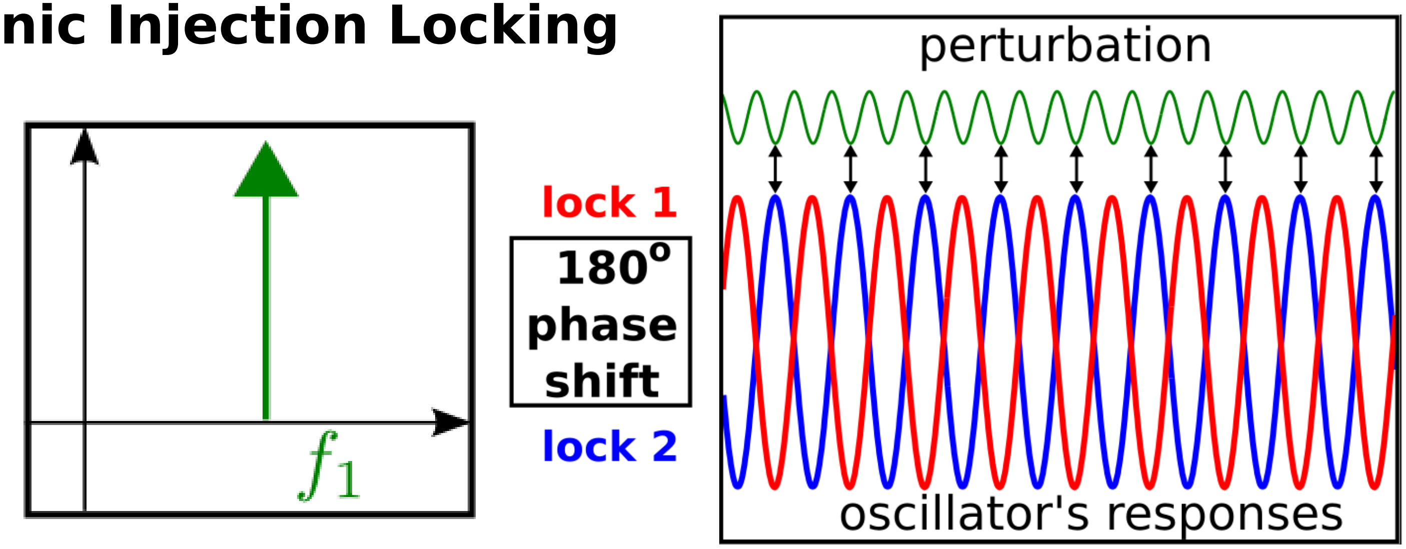
  - **we use a variant: sub-harmonic injection locking**
    - details: Neogy/Roychowdhury, "Analysis and design of sub-harmonically injection locked oscillators", Proc. DATE, March 2012.

Underlying Mechanism: Injection Locking

Injection Locking

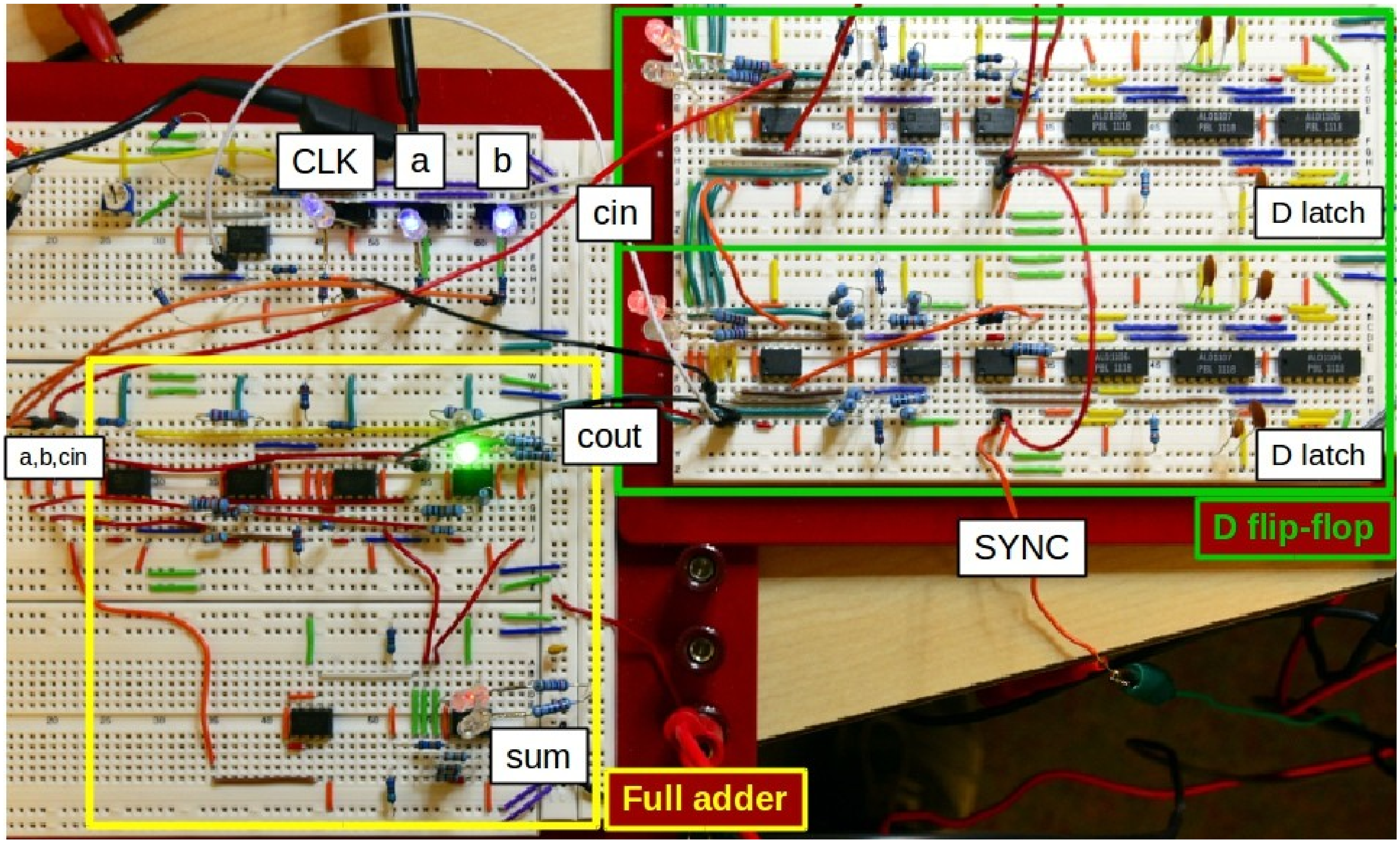


Sub-harmonic Injection Locking (SHIL)



First Phase Logic FSM with Oscillators

- **PHLOGON** with **CMOS ring oscillators**



details: Wang/Roychowdhury, “PHLOGON: PHase-based LOGic using Oscillatory Nano-systems”. UCNC, 2014.

What's needed for designing PHLOGON systems?

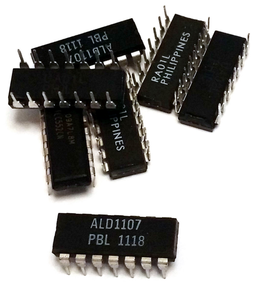
Compact models

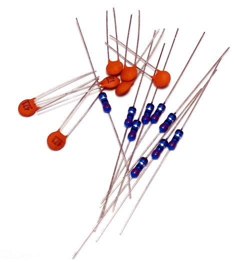
easy to write
new models

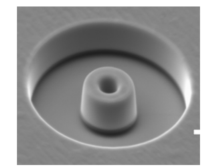
MAPP

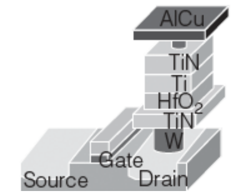
easy to prototype
specialized algorithms
for oscillator-based
systems

Specialized design tools

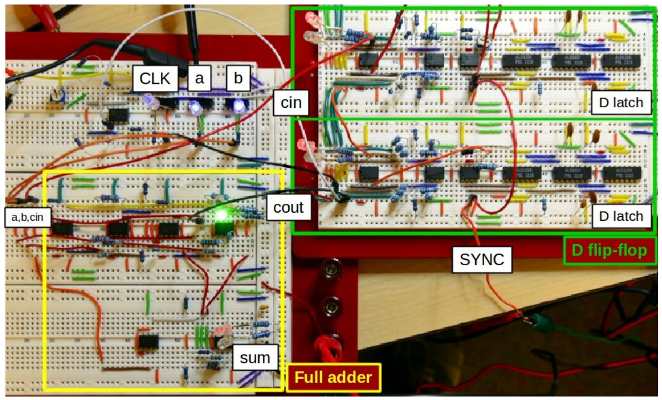




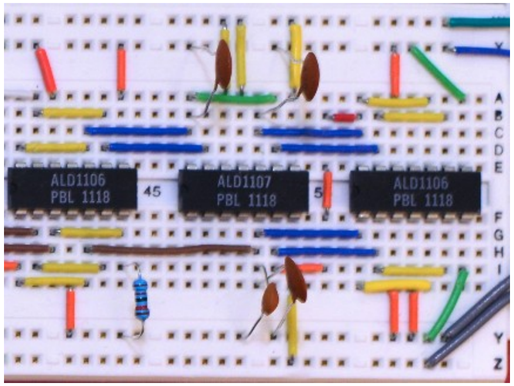


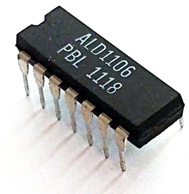


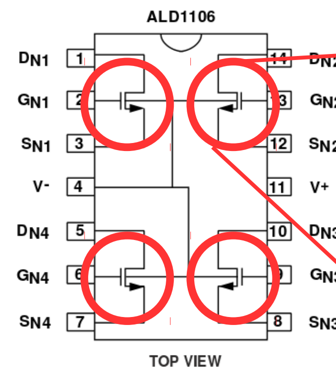
Oscillator-based Boolean computing systems



Modelling CMOS Ring Oscillators in MAPP

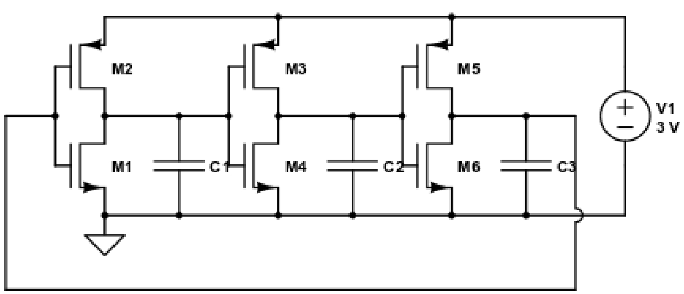






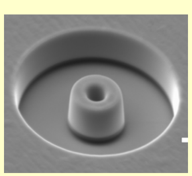

```
.MODEL ALD1106 NMOS (LEVEL=1
          + CBD=0.5p
          + CBS=0.5p
          + CGDO=0.1p
          + CGSO=0.1p
          + GAMMA=.85
          + KP=225u
          + L=10E-6
          + LAMBDA=0.029
          + PHI=.9
          + VTO=0.7
          + W=20E-6)
```

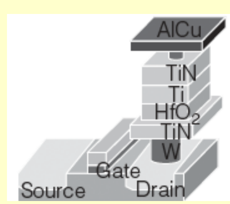
SPICE MOS level 1 model



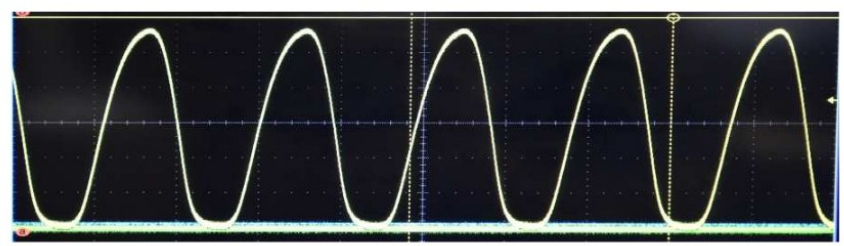
CMOS ring osc.

few days to implement in MAPP

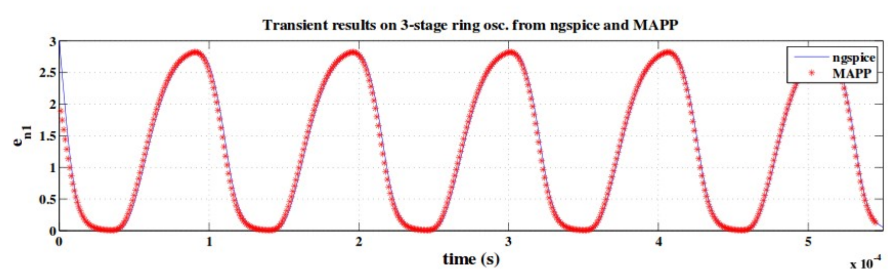




...

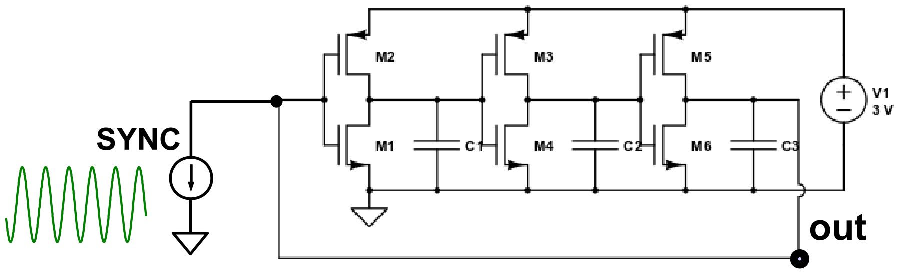


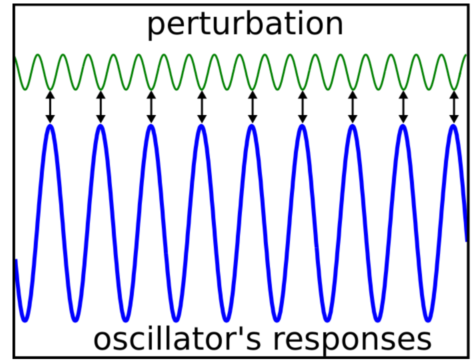
(a) Results seen from an oscilloscope.



(b) Simulation results from ngspice and MAPP.

Simulating SHIL of Oscillators

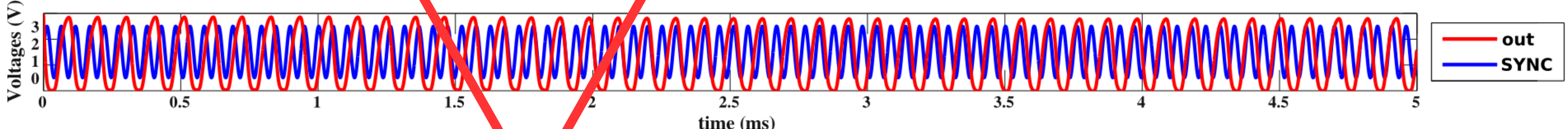




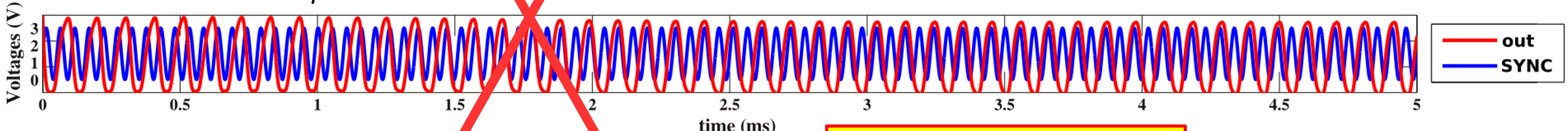
Sub-harmonic Injection Locking (SHIL)

Standard SPICE transient simulation

Is SHIL happening with 20 μA SYNC?

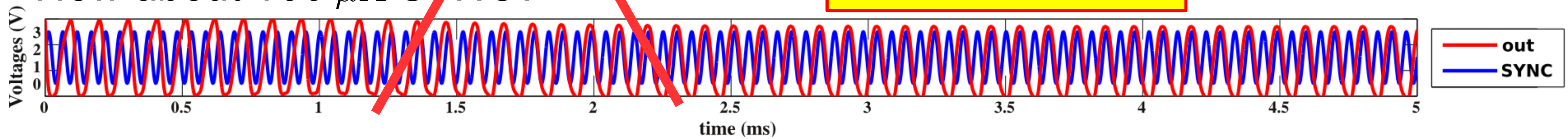


How about 50 μA SYNC?



hard to observe SHIL

How about 100 μA SYNC?



inefficient

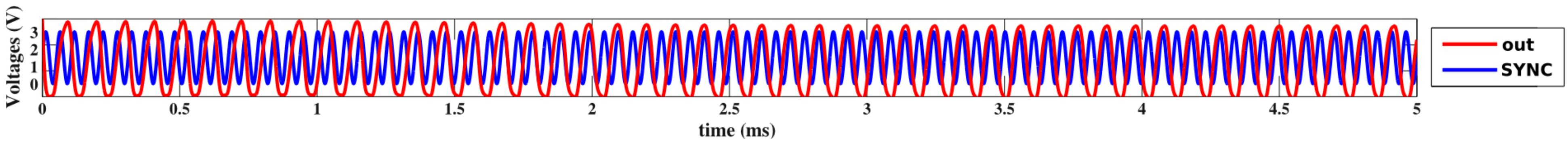
unbounded error in phase

not much insight into design

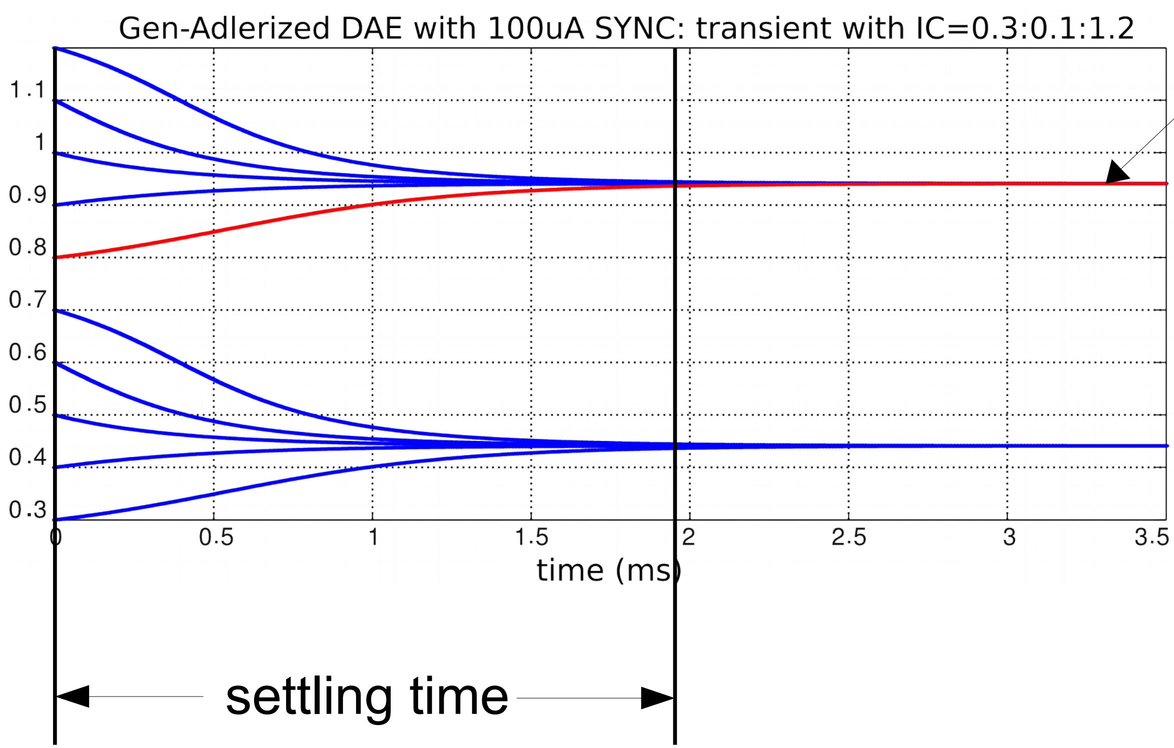
Phase macromodel analyses in MAPP

Phase-macromodel-based analyses in MAPP

Standard SPICE transient simulation



Phase-based simulation in MAPP



SHIL occurs: curve "flattens"

"locked phase error"

$\Delta\phi$

Generalized Adler's Equation

$$\frac{d}{dt}\Delta\phi(t) = f_0 - f_1 + f_0 \cdot g(\Delta\phi(t))$$

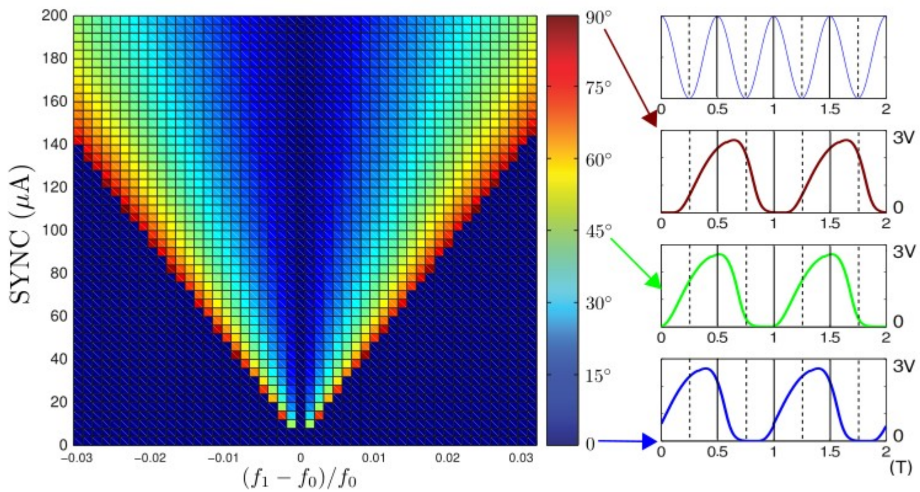
$$g(\Delta\phi(t)) = \int_0^1 \vec{v}_1^T(\tau + \Delta\phi(t)) \cdot \vec{b}_1(\tau) d\tau$$

Perturbation Projection Vector (PPV)

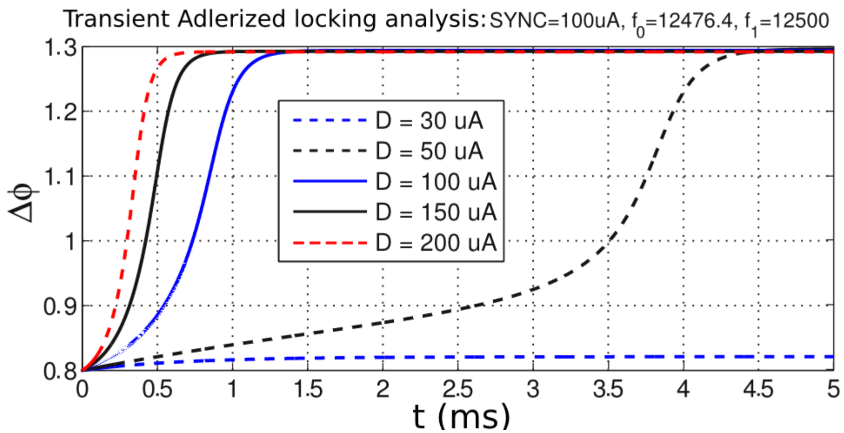
details: Bhansali/Roychowdhury, "Gen-Adler: the Generalized Adler's equation for injection locking analysis in oscillators". Proc. ASPDAC, 2009.

More MAPP Capabilities

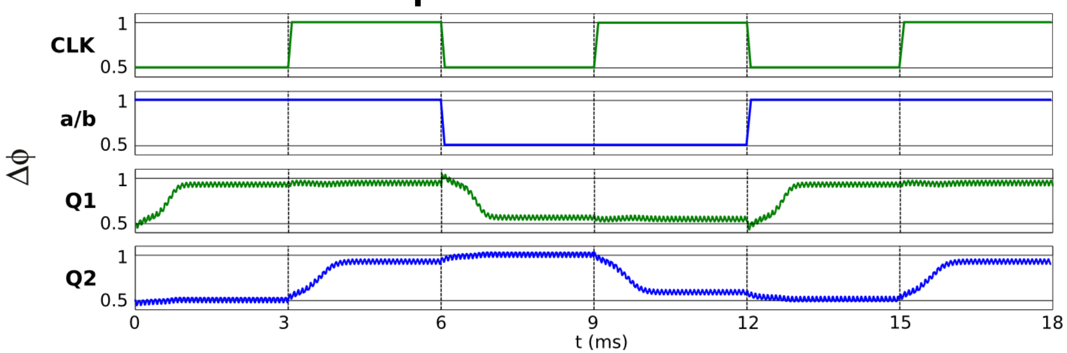
Locked phase error vs. variations in oscillator natural frequency



Timing of phase-based D latch



Full system transient in phase domain

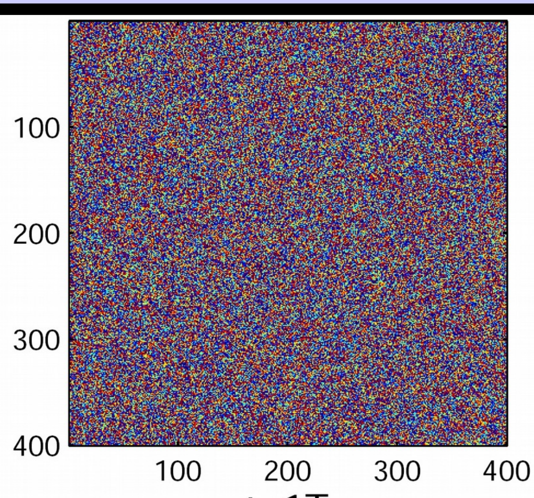


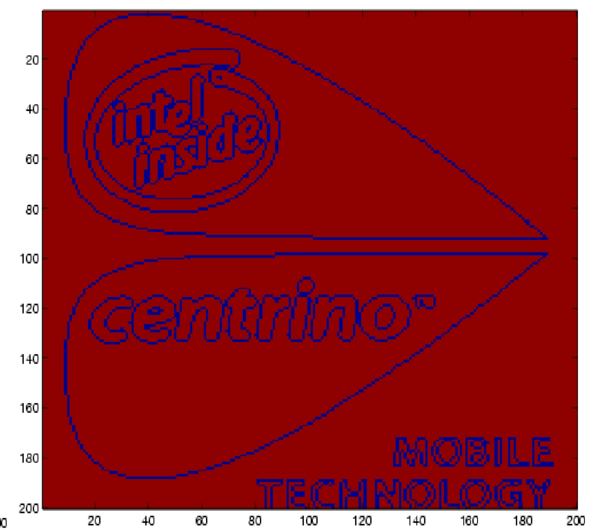
details: Wang/Roychowdhury, "Design Tools for Oscillator-Based Computing Systems". Proc. DAC, 2015.

The role of NEEDS in PHLOGON

- **MAPP enables prototyping novel design tools**
  - easy to insert compact models for novel nanodevices
    - and debug them and get them to work properly in simulation!
  - easy to write specialized algorithms/tools for oscillatory systems
    - regular SPICE simulation: slow, inaccurate, little insight

Coupled Oscillator Network

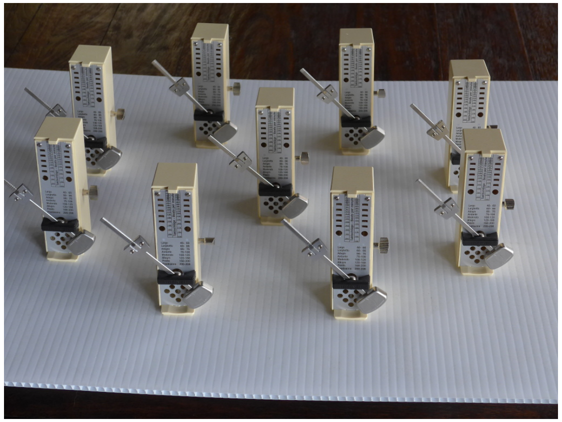


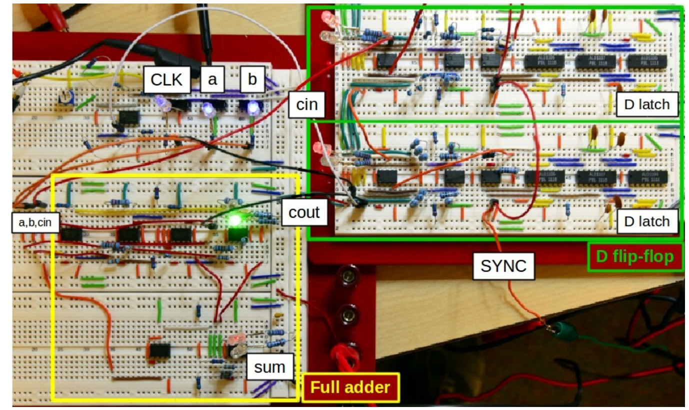


~1200x faster than SPICE-level

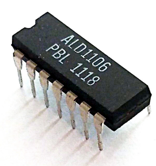
- details: Lai/Roychowdhury, “Fast Simulation of Large Networks of Nanotechnological and Biochemical Oscillators for Investigating Self-Organization Phenomena”, Proc. ASPDAC, 2006.

Summary

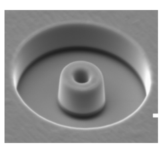


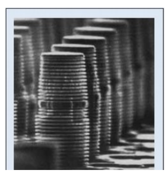


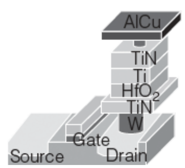
CLK
a
b
cin
D latch
a,b,cin
cout
D latch
SYNC
D flip-flop
sum
Full adder



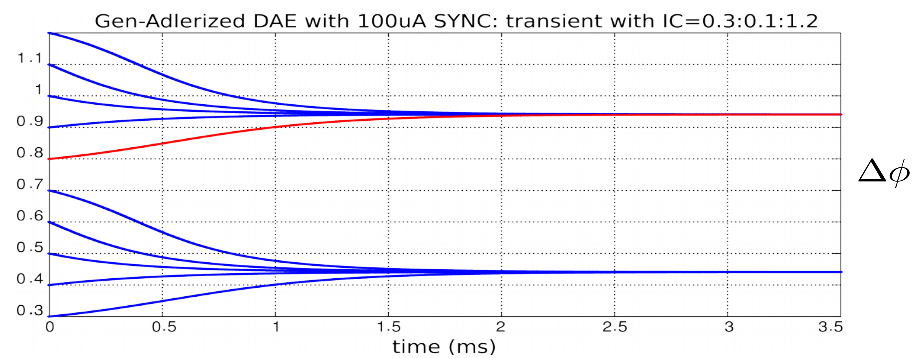
ALD1106
PBL 1118



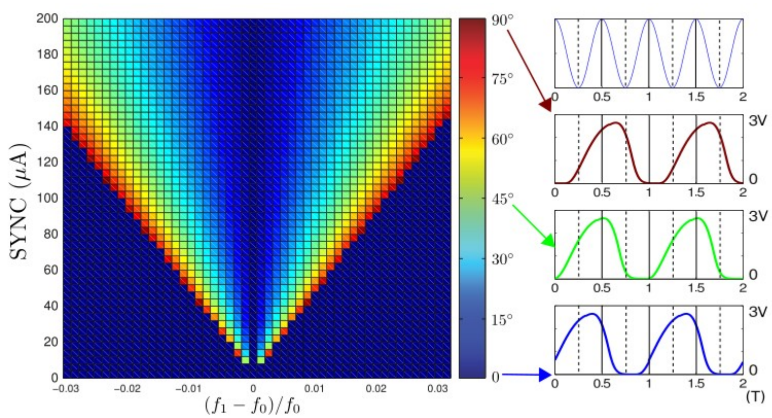




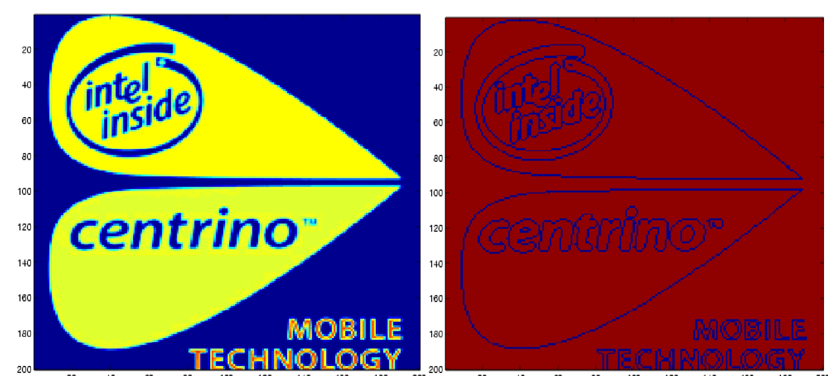
AlCu
TiN
Ti
HfO2
TiN
W
Gate
Source
Drain



Gen-Adlerized DAE with 100uA SYNC: transient with IC=0.3:0.1:1.2
time (ms)
$\Delta\phi$



SYNC (μA)
$(f_1 - f_0)/f_0$
90°
75°
60°
45°
30°
15°
0
3V
0
(T)



intel inside
centrino
MOBILE
TECHNOLOGY