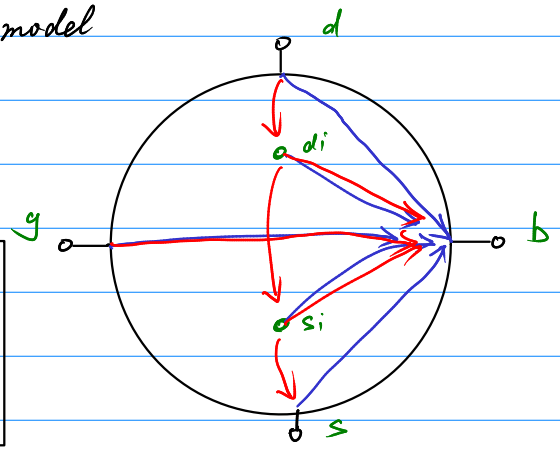
MVS 1.0.1 Verilog A → ModSpec → MDE

Outline :

① Convert MVS VA to ModSpec (manually)

- analyse VA model



VA (Udb, Vgb, Vsb, Vdib, Vsib)
= (Iddi, Idisi, Isis
Qgb, Qdib, Qsib)

ModSpec
- terminals d g s b
- explicit outs $\begin{bmatrix} idb \\ igb \\ isb \end{bmatrix}$
- parms
- internal unks $\begin{bmatrix} Vdib \\ Vsib \end{bmatrix}$

$$-\begin{bmatrix} idb \\ igb \\ isb \end{bmatrix} = \vec{fe} + \frac{d}{dt}\vec{qe} = \begin{bmatrix} Iddi \\ 0 \\ Isis \end{bmatrix} + \frac{d}{dt}\begin{bmatrix} 0 \\ Qgb \\ 0 \end{bmatrix}$$

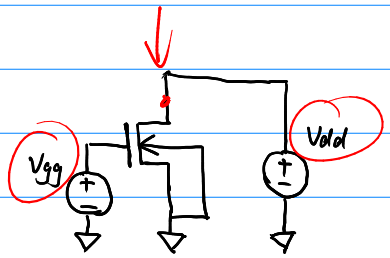
$$\underset{di\ si}{KCLs} : \vec{0}\Big|_2 = \vec{fi} + \frac{d}{dt}\vec{qi} = \begin{bmatrix} -Iddi - Idisi + \frac{d}{dt}Qdib \\ Idisi + Isisi + \frac{d}{dt}Qsib \end{bmatrix}$$

- look at ModSpec model

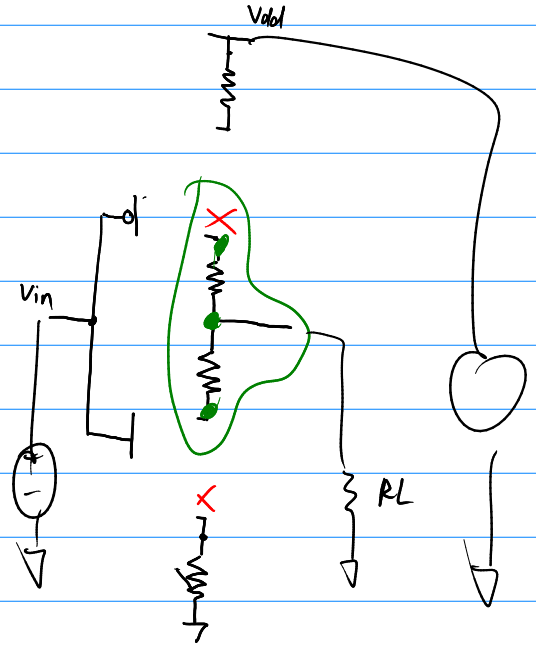
② Run functions in ModSpec model

③ Run circuits in MDE

- characteristic curves

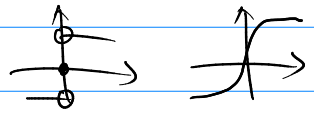


- inverter



- ring oscillator

→ Questions : Why does it work in HSPICE

① absc, derivatives smoothing 

② clkTgmin → SPICE code

builtin

③ fetlim → init / limiting

builtin

④ analysis not standard NR

④ Summary

- Verilog A → use branches, continuous, smooth
- check f / q, df / dq at the ModelSpec level
- Convergence :
  - stay connected : gmin
  - init / limiting